

M.S. ENGINEERING COLLEGE

Navarathna Agrahara, Sadahalli Post, Bangalore -562110



ANALOG ELECTRONIC CIRCUITS LAB MANUAL (As Per VTU Syllabus – 2012)

Dept Of Electronics & Communication Engineering

PREPARED BY :

Chaluva Raju R , Asst. Professor.

Savitha S C , Asst. Professor.

APPROVED BY :

Venkateshappa

Assc. Professor & HOD

Course Syllabus (As Per VTU)

1. Wiring of RC coupled single stage FET amplifier and determination of the gain-frequency response, input and output impedances.
2. Wiring of RC coupled single stage BJT amplifier and determination of the gain-frequency response, input and output impedances.
3. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances(single circuit)(one experiment)
4. Wiring and testing for the performance of BJT-RC phase shift oscillator for $f_o \leq 10 \text{ KHz}$.
5. Testing for the performance of BJT-Hatley and Colpitts oscillators for RF range $f_o \geq 100 \text{ KHz}$.
6. Testing for the performance of BJT-crystal oscillators for $f_o \geq 100 \text{ KHz}$.
7. Testing of diode clipping (single/Double ended) circuits for peak clipping, peak detection.
8. Testing of clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less class-B push pull power amplifier and determination of its conversion efficiency.
10. Testing of half wave, full wave and bridge rectifier circuits with and without capacitor filter. Determination of ripple factor, regulation and efficiency.
11. Verification of Thevinin's Theorem and maximum power transfer theorem for DC circuit.
12. Characteristics of Series and Parallel Resonant Circuits

CYCLE OF EXPERIMENTS

CYCLE – I	
1.	Testing of Diode Clipping Circuits a. Single ended positive and negative clipping (Shunt(parallel)) b. Double ended clipping (Symmetrical & Asymmetrical)
2.	Testing of Diode Clamping Circuits :-Positive clamping & Negative clamping
3.	Characteristics of Resonant Circuits a) Series resonant a) Parallel resonant
4.	Testing of Rectifier circuits & determine Ripple factor, Regulation, Efficiency for a) Half wave rectifier with and without filter. b) Full wave center tapped rectifier with and without filter c) Full wave bridge rectifier with and without filter
5.	Wiring of RC coupled single stage amplifier & determine the gain, frequency response, input & output impedances (With BJT or FET)
6.	Wiring & testing for the performance of Oscillator for RF oscillator for RF range $f_0 = 100\text{kHz}$. a) Hartley oscillator & b) Colpitts oscillator
CYCLE II	
7.	Wiring & testing for the performance of BJT-RC phase shift oscillator for range $f_0 = 10\text{kHz}$
8.	Wiring of a two stage BJT voltage series feedback amplifier and determine the gain, frequency response, input & output impedances a) With the Feedback & b) Without the feedback.
9.	Verification of Thevenin's Theorem and Maximum Power Transfer theorem for DC circuits.
10.	Wiring of BJT Darlington Emitter follower & determine the gain, input & output impedances with & without bootstrapping.
11.	Testing of a transformer less Class –B push pull amplifier and determine its conversion efficiency.
12.	Testing for the performance of BJT – crystal oscillator for $f_0 > 100\text{kHz}$.

CONTENTS

Sl No.	TOPICS	Page No
1.	INTRODUCTION	1
	EXPERIMENTS	
2.	RC coupled single stage BJT Amplifier	10
3.	RC coupled single stage FET Amplifier	18
4.	BJT Darlington Emitter Follower with and without bootstrapping	23
5.	BJT-RC Phase Shift Oscillator	30
6.	BJT-Hatley and Colpitts Oscillators	35
7.	BJT-Crystal Oscillator	44
8.	Diode Clipping (single/Double ended) Circuits	48
9.	Diode Clamping circuits	59
10.	Class-B Push Pull Power Amplifier	64
11.	Half wave, Full wave and Bridge Rectifier Circuits	68
12.	Thevinin's Theorem and Maximum Power Transfer Theorem	93
13.	Series and Parallel Resonant Circuits	100
14.	MODEL QUESTION BANK	108

INTRODUCTION

OVERVIEW OF ANALOG ELECTRONIC CIRCUITS LABORATORY

Analog Electronics as the name suggests deals mainly with processing of Analog signals. Analog electronic circuit design is one of the important and challenging field in Electronics. The area of analog electronics is one of the vast and complex areas in VLSI circuits design. A signal which is having different values at different instants of time and having its value defined at every instants of time is referred to as an analog signal. Circuits to process analog signals are necessary because all the naturally available signals like human speech, sound ,biomedical, temperature etc are analog in nature. Analog electronic circuits can be designed and tested for their performance using the CAD tools like PSPICE, Cadence, etc.. Many analog circuits are available in the form of IC chips.

During this Lab course simple analog electronic circuits are designed using discrete components like Resistors, Capacitors, Inductors, PN junction diodes and Transistors (BJT's, FET's, etc.). These designed circuits are tested and verified for their performance under the laboratory conditions using power sources like DC Power supply, AC sources like function generators. Their input and output parameters like input waveforms, output waveforms, input and output current and voltage readings, the impedance or resistance offered by the circuit, etc are analyzed by using measuring instruments like multi-meter and CRO's. The captured values from the instruments are noted and used for further calculations.

Similar to Analog electronics, we have Digital electronics which mainly deals with digital circuit design. A Digital signal can be represented by using only two values 0 or 1 at any instant of time. Logic gates, Flip-Flops, Registers, etc are some examples of basic digital circuits. Digital circuits are mainly classified as Combinational and Sequential circuits. The experiments on these circuits will be dealt in logic design laboratory.

All the signals are basically analog signals. So there exists need for converting an Analog signal to a Digital signal or vice versa. Analog to Digital converters (ADC's) and Digital to Analog converters (DAC's) with different specifications are available for this purpose. Digital signal processing is fast compared to the processing of analog signals. So in most of the applications the input analog information is converted to its digital equivalent and there after the digital equivalent of the analog signal is processed. It is again converted back to its analog form to retrieve the original analog signal. A simple and popular example is MP3 format representation of the audio signals which are basically analog in nature, i.e. the audio or speech signals. Both analog and digital electronics play an important role in the field of – Electronics and communications.

Digital electronics field is like a catalyst for processing analog signals with desired and designed levels of accuracy.

ANALOG ELECTRONICS LABORATORY COURSE FLOW:

This laboratory course completely deals with basics of analog electronic circuit design and their experimental observations. Here the students are exposed to design and implement the analog circuits like Clipping and Clamping circuits using diodes, Amplifiers using FET's or BJT's, verification of circuit theorems such as Thevenin's and maximum power transfer theorems, behavior of RL, RLC circuits, oscillators such as RC phase shift, Hartley, Colpitt's and Crystal oscillators, full wave and half wave rectifier circuits, resonance circuits, etc..

To start with this laboratory session, initially all students are trained to use the measuring instruments like Multi-meter and CRO. Thorough understanding of CRO is mandatory for proceeding with the course wear. The function or signal generators which generate the analog signals of desired frequency and amplitude (frequency and voltage levels) are made familiar to the students. Reading the values of the passive components like resistor, capacitor, etc. using color code are taught.

After completing the above exercise, the design aspects of analog circuits are carried out. Thereafter the conduction of the experiments are started to verify and test the performance of the designed analog circuits. The input and generated output waveforms are sketched and the results are noted for further calculations.

Instructions to the students are given in the start of this document which they are advised to read before they start conducting experiments.

INSTRUCTIONS BEFORE STARTING THE EXPERIMENT

1. Study the circuit, theory and procedures, expected output before doing the experiment.
2. Get familiarize with the components and equipments used in the lab, Ex: Resistors, Capacitors Inductors, Signal generators, BJTs, FETs, CROs, Digital Multi-meter etc.

3. RESISTORS

The Resistors used in this lab are of two types, (1)fixed value resistors which have colour bands and (2) Variable value resistors (Decade Resistance Box(DRBs)).

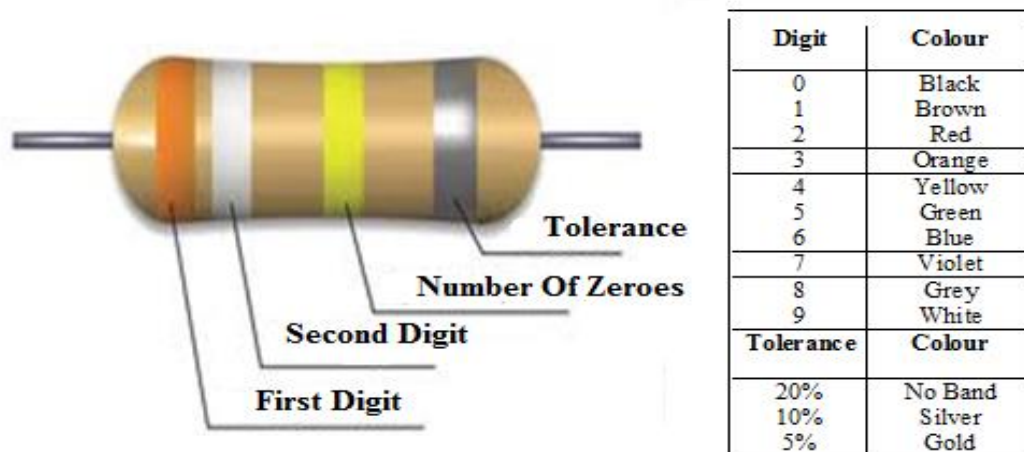


Fig 1. A fixed value resistor

Table 1. Colours with Digits

A Fixed value resistor looks as shown in the above image. The value of this kind of resistors is determined as shown below.

We have to start from the side opposite to the gold or silver colour and go left to right. Now the Value of Resistor=(First colour digit)(Second colour digit)(That many zeroes as third colour digit) ±

(Fourth colour) ohms

$$=(\text{First Digit})(\text{Second Digit})(\text{Number of Zeroes}) \pm (\text{Tolerance}) \Omega$$

For example ,if for a given resistor ,first colour is **Brown** ,second colour is **White**, third colour **Yellow** and fourth colour is **Silver**, then the value of this resistor is determined using Table 1 and above equation as,

$$\text{Value of resistor} = (\text{First Digit})(\text{Second Digit})(\text{Number of Zeroes}) \pm (\text{Tolerance}) \Omega$$

$$= (1) (9) (0000) \pm 10\%$$

$$= 190000 \pm 0.1$$

$$\approx 190 \text{ K}\Omega \text{ (neglecting tolerance)}$$

Note : Finding the value of a variable value resistor (DRB) is straight forward in which we will set the value using knobs provided on the DRBs. The value of the resistor is sum of the values shown by each knob.

4. CAPACITORS



Fig 2 . Ceramic Capacitor

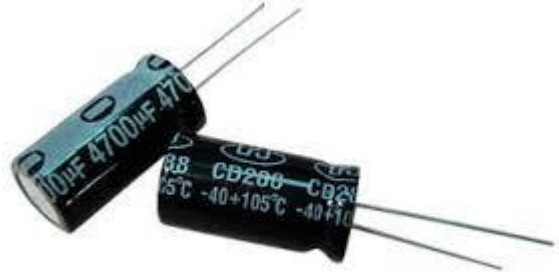


Fig 3. Electrolytic Capacitor

Capacitors are of two types , (a) Ceramic capacitor and (b) Electrolytic capacitors .They look like as shown in Fig 1 and Fig 2 given above.

(a) Ceramic Capacitor : Ceramic capacitors have no polarity and the value of these capacitors is

determined by using the digits shown on their body in fig 2, as follows ,

Value of capacitor= (First two digits)(That many Zeroes as third digit) pico farads

For example. if the digits shown on the capacitor is **154** , then its value is determined as ,

Value of capacitor = (First two digits)(That many Zeroes as third digit) pico farads

$$= (15) (0000) \text{ pF}$$

$$= 150000 \times 10^{-12} \text{ F (since pF} = 10^{-12} \text{ F)}$$

$$= 15 \times 10^4 \times 10^{-12} \text{ F}$$

$$= 15 \times 10^{-8} = 0.15 \times 10^{-6} = \mathbf{0.15 \mu F}$$

(b) Electrolytic Capacitor : Electrolytic Capacitors have polarities ,so their terminals are represented as positive and negative terminals that we can identify by seeing the body of

the capacitor that appears as shown in Fig 2 given above. Usually the lengthier terminal is the positive terminal and shorter terminal is the negative terminal. The value of the capacitor is given on the body of the capacitor itself.

5. SIGNAL GENERATOR AND ITS ADJUSTMENTS

Signal generator or Function generator is an electronic instrument which is used as AC signal source to give AC input signals of different shapes (square wave ,sine wave ,etc) and wide range of frequency required by the circuit. It has Voltage and Frequency knobs to adjust Voltage and Frequency of the input AC signals.



Fig 4. Signal or Function generator

Before connecting the signal generator to the circuit check the followings

- a. Set the shape of the waveform (sinusoidal).
- b. Set the frequency using coarse and fine adjustments.
- c. Set the offset adjustments. Set the CRO in DC mode and ensure the waveform is symmetry in both positive and negative cycle. If not , adjust it using the DC offsetting potentiometer
- d. Set the Voltage magnitude using Vcoarse settings and Vfine adjustments.

6. CRO (CATHODE RAY OSCILLOSCOPE) AND ITS ADJUSTMENTS

CRO (Cathode Ray Oscilloscope) is an electronic instrument used to display ,observe and analyse the outputs of the circuits. It has two channels two display two different outputs. Each channel has two axis ,vertical axis which represents amplitude and horizontal axis which represents time. Values of amplitude and time of the signal are measured by using corresponding amplitude and time knob(which is common for both channels) on the CRO for both channels.

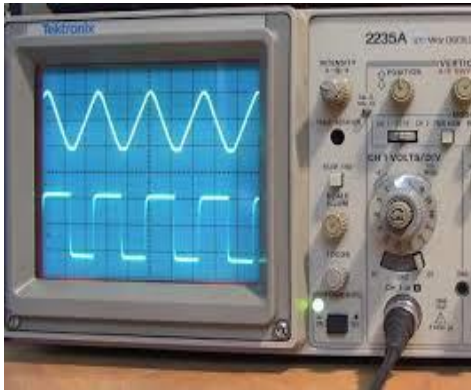


Fig 5. Cathode Ray Oscilloscope

- Select the right voltage and time scale to get the proper waveform
- For clipper and clamper circuits, observe the waveform in DC mode only
- Set the input waveform mainly for offset setting in DC mode only.
- Before measurement, ensure X & Y are in calibrated mode (if provided externally)
- Ensure that Channel selection and trigger mode are properly set.
- In case of two channels do not mix the signal and ground terminals.

7. MULTI-METER ADJUSTMENTS



Fig 6. Multi Meter

- Set the right mode before taking the readings. Wrong mode settings may damage the instrument.
- For current reading, connect the multi-meter in mA (or A) mode to the circuit before switching on the supply. Do not remove the current meter when the supply is on. Check for ac and dc modes as required.
- Use the proper probes for the measurement. Wrong cables may damage the instrument.

8. IDENTIFICATION OF TRANSISTOR TERMINALS



Fig 7. Transistor

Hold the Transistor as shown in Fig 7 given above . From the notch or Tab in the anticlockwise direction, **first** is **Emitter** , **middle** one is **Base** and the last i.e. **third** terminal is **Collector** terminal.

9. VOLTAGE REGULATED POWER SUPPLY (VRPS) (Dual D.C Power Supply)



Fig 8. Voltage Regulated Power Supply

VRPS is used to provide D.C power required by the circuit if any and it looks as shown in Fig 8

10. BREAD BOARD

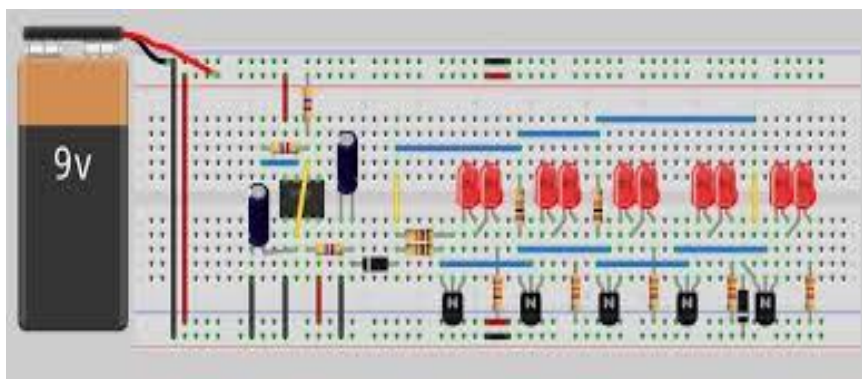


Fig 9. Bread Board

Bread Board is apparatus which is used as the base to connect components of the circuit as shown in the Fig 9. Bread Board has connections points which are divided into rows and columns which in turn are internally shorted.

11. After adjusting the input voltage, check the circuit connections before turning the power on.

12. The ground connections are made properly & ensure that the circuit has one ground.

13. Connect the ground terminal of signal generator and the oscilloscope to the same point. Do not mix the ground point and signal of the two instruments to get the proper readings.
14. Don't pull out the connections with the power supply on.
15. Use only stripper to remove insulation.
16. Don't short the terminals while checking the output at pin terminals.
17. Don't switch on supply to the circuit unless the staff has checked the circuit connections.

EXPERIMENT NO. 1(A)**RC COUPLED SINGLE STAGE BJT AMPLIFIER****AIM**

To design RC Coupled single stage BJT amplifier for the given values of V_{CE} and I_C and to determine the gain, frequency response, input and output impedances.

COMPONENTS REQUIRED

Sl. No	Apparatus and components	Range	Quantity
1	Bread Board		1
2	NPN transistor	SL100	1
3	Resistors	270 Ω , 4.7K Ω , 22K Ω , 1K Ω	1 each
4	Capacitors	0.47 μ F, 50 μ f	2+1
5	VRPS	0-30V DC, 3A	1
6	Signal generator	10Hz to 3MHz	1
7	CRO for testing		1
8	Probes, wires		2+15
9	DRB	0 to 1M Ω	1
10	Digital multimeter		1

THEORY

Amplifier circuit is used to enhance or amplify the input signal level. RC coupled amplifier is most popular type of coupling because it provides excellent audio fidelity over wide range of frequencies. Coupling is used to couple alternative input & output signal with DC biased transistor device or any other device used for amplification.

It is usually employed in voltage amplification this type of amplifier uses resistance as load in the collector circuit and capacitor elements for coupling input and output. Coupling capacitor is used to couple ac signal to the dc biased transistor circuit. RC coupled amplifier has large bandwidth. Circuit diagram 1.a shows the single stage of an RC coupled amplifier. The resistance R_1 , R_2 and R_E form the biasing and stabilization network. The emitter bypass capacitor offers low reactance path to the a.c input signal, without it, the voltage gain of each stage would be lost. The coupling capacitors at the input and output of transistor transmits a.c signal but blocks d.c. This prevents d.c interference between various stages and the shifting of operating point.

There is a 180 degree phase shift between input and output of the amplifier because, an increase in input voltage causes the base current to increase, which results in increased collector current which further results in an increased voltage drop across the load resistor and a decreased collector voltage. Hence there is a 180 degree phase shift between input and output amplifier.

CIRCUIT DIAGRAM

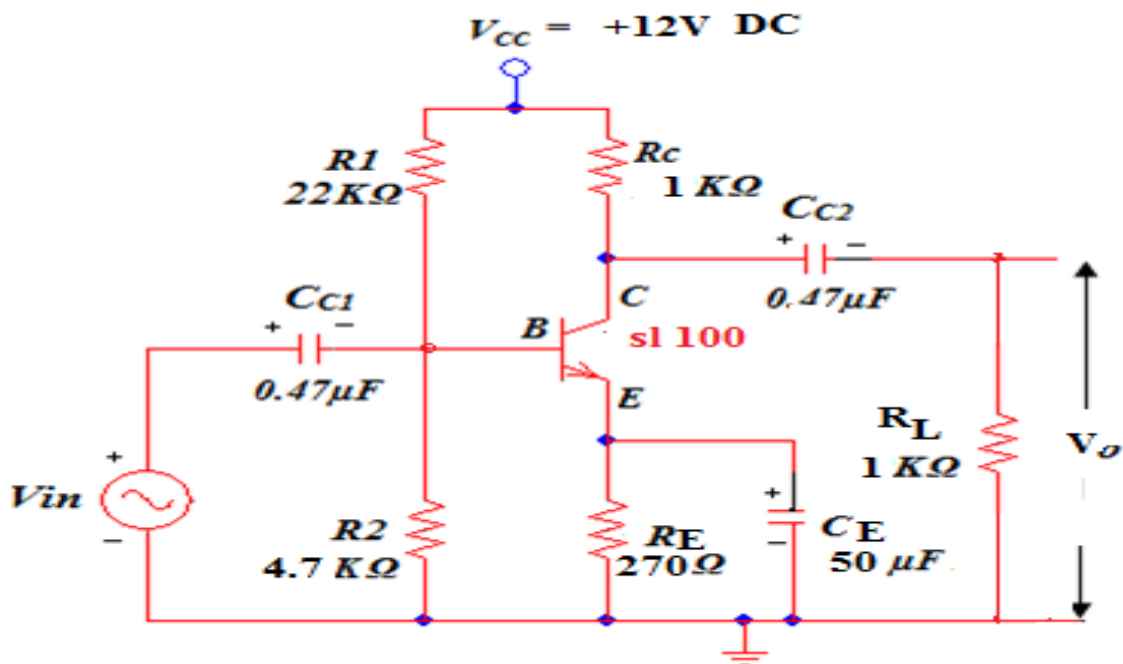


Fig 1(A).a - RC coupled amplifier

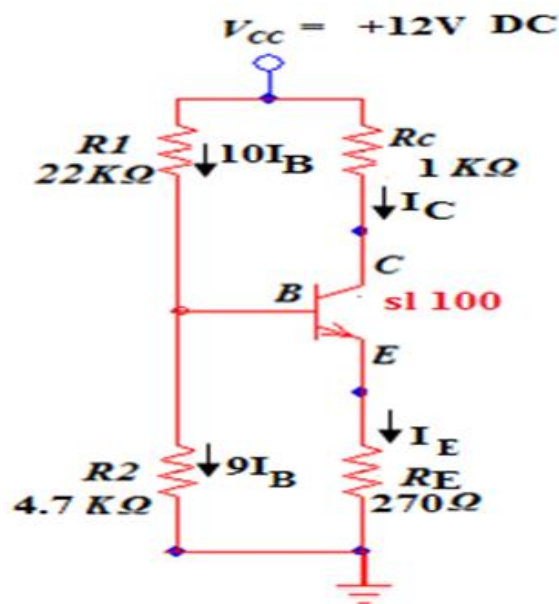


Fig 1(A).b – Biasing Circuit

DESIGN

Given: $V_{CC}=12\text{ V}$, $I_C=4.5\text{ mA}$, $\beta=100$ (for SL 100)

Assume $V_{RE}=V_E=V_{CC}/10=12/10=1.2\text{ V}$

To find R_E :

$$R_E=1.2/I_C=1.2/4.5\text{mA}$$

$$=0.267\text{ K ohm}$$

$$\mathbf{R_E=270\Omega}$$

To find R_C :

Choose $V_{CE}=V_{CC}/2=12/2=6\text{ V}$

Apply KVL in CE loop:

$$V_{CC}-(I_C R_C)-V_{CE}-V_{RE}=0$$

$$12-(4.5R_C)-6-1.2=0$$

$$R_C=1.07\text{ K ohm}$$

$$\mathbf{R_C=1\text{ K }\Omega}$$

To find R_1 & R_2 :

$$V_B = V_{BE} + V_{RE}$$

$$V_B = 0.7 + 1.2 = 1.9\text{V}$$

$$I_C = \beta I_B$$

$$I_B = I_C / \beta = 4.5\text{mA} / 100 = 0.045\text{mA}$$

Assume $10I_B$ flows through R_1 and $9I_B$ flows through R_2

$$R_1 = (V_{CC} - V_B) / 10 I_B = 22.7$$

$$\mathbf{Use\text{ }R_1=22\text{K}\Omega}$$

$$\mathbf{R_2= V_B/9I_B=4.69K\Omega}$$

$$\mathbf{Use\text{ }R_2=4.7\text{K}\Omega}$$

To find C_E

Let $f_L=500\text{Hz}$ (Lower Cut-off frequency)

$$f_L = 1 / 2\pi * R_E * C_E$$

$$\text{But } R_E \approx r_e \quad \text{Here } r_e = V_T / I_C = 26\text{mV} / 4.5\text{mA} = 5.77\Omega$$

$$R_E \approx r_e \approx 6\Omega$$

$$1/(2\pi f_L C_E) = R_e$$

$$\text{Therefore, } C_E = 1/(2\pi \cdot 500 \cdot 6)$$

$$C_E = 53 \mu\text{F}$$

Use $C_E \approx 50 \mu\text{F}$

To design Cc1

$$f_L = 1 / (2\pi (R_i/10) C_{c1})$$

$$R_i = R_1 \parallel R_2 \parallel h_{ie} \quad \text{Where } h_{ie} = \beta \cdot r_e$$

$$\text{For SL100 } \beta = 150 \text{ and Let } r_e = 10\Omega, h_{ie} = 150 \cdot 10 = 1.5\text{K}\Omega$$

$$R_i \approx h_{ie} = 1.5\text{K}\Omega$$

$$\text{So } C_{c1} = 1 / 2\pi R_i f_L = 1 / (2\pi \cdot 0.15\text{K}\Omega \cdot 500) = 2.12 \mu\text{F}$$

To design Cc2

$$\text{Let } R_L = 1\text{K}\Omega$$

$$f_L = 1 / (2\pi ((R_o + R_L)/10) C_{c2})$$

$$\text{For the above circuit } R_o = R_c = 1\text{K}\Omega \text{ and let } R_L = 1\text{K}\Omega$$

$$\text{So } C_{c2} = 1 / (2\pi \cdot 0.2\text{K}\Omega \cdot 500) = 1.59 \mu\text{F}$$

Use $C_{c1} = C_{c2} = 0.47 \mu\text{F}$ (ceramic)

PROCEDURE

Rig up the circuit as shown in the circuit diagram in Fig 1(A).b without connecting signal generator. Check the biasing conditions i.e. $V_{CC} = 12\text{V}$ and check corresponding values of V_{CE} , V_{BE} , V_E .

1. Connect the as in Fig 1(A).a with signal generator and designed capacitor values and set the input voltage constant at 50mV(p-p) , 1KHz .
2. Now vary the input frequency starting from 100Hz to MHz range and note the corresponding output voltage(peak to peak).
3. Plot the graph of frequency v/s output voltage gain in decibel with frequency on X-axis and dB gain on Y-axis and determine the bandwidth.

TO DETERMINE INPUT IMPEDANCE (Z_i) AND OUTPUT IMPEDANCE (Z_o)

(a) INPUT IMPEADNCE (Z_i)

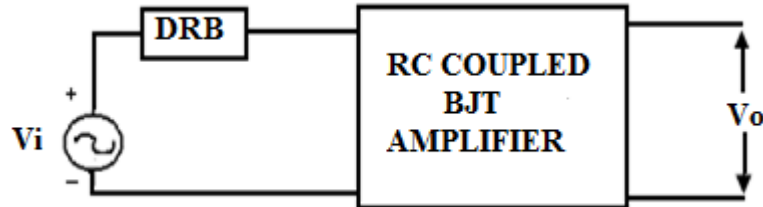


Fig 1(A).c -Circuit to find the input impedance

PROCEDURE

1. Connect the circuit as shown in the Fig 1(A).c to obtain input impedance and set the input frequency at say 10kHz(center frequency).
2. Set the DRB value to minimum initially and note the corresponding output voltage. Start increasing the resistance in the DRB from the minimum value until output voltage becomes half. when the output voltage becomes half of the initial value, the corresponding resistance in the DRB is the input impedance(Z_i).

(b) OUTPUT IMPEDANCE (Z_o)

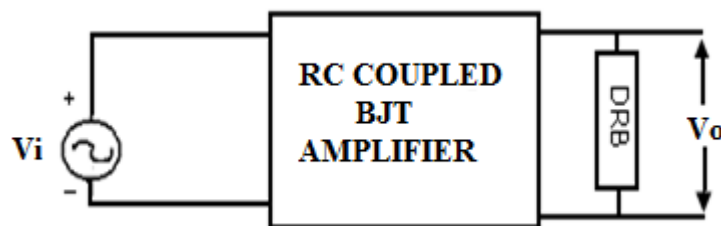


Fig 1(A).d - Circuit to find the output impedance

PROCEDURE

1. Connect the circuit as shown in the diagram 1(A).d to obtain output impedance and set the input frequency at say 10kHz(center frequency).
2. Set the DRB value to maximum initially and note the corresponding output voltage. Start decreasing the resistance in the DRB from the maximum value until output voltage becomes

half. When the output voltage becomes half of the initial value, the corresponding resistance in the DRB is the output impedance (Z_o).

EXPECTED GRAPH OF FREQUENCY RESPONSE

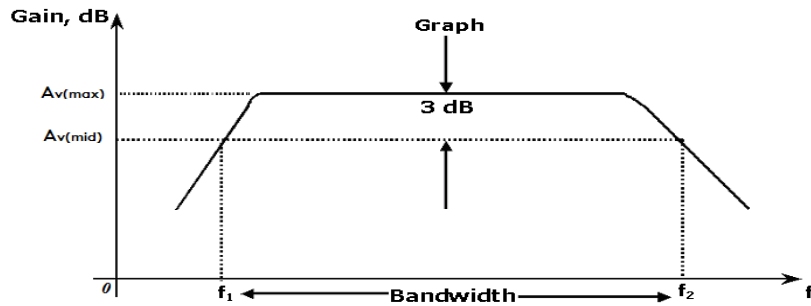


Fig 1(A).e- Frequency response curve of RC coupled amplifier

TABULAR COLUMN

Frequency f (Hz)	Output voltage (V _{O(P-P)}) Volts	Voltage Gain V _o / V _i	Gain(dB) = 20 log (V _o / V _i)

--	--	--	--

Table 1(A).a To record observed values.

RESULT

The RC Coupled Amplifier was designed and the values of following quantities are observed and compared with theoretical values .

Midband Voltage Gain =

Midband Voltage Gain in dB =

Lower Cut-off Frequency =

Upper Cut-off Frequency =

Bandwidth (BW) =

Input Resistance (Z_i) =

Output Resistance (Z_o) =

EXPECTED VIVA QUESTIONS

1. What is a transistor? What the name transistor stands for ?.
2. What the names BJT and FET stands for ? What is the difference between BJTs and FETs?.
3. What do you mean by transistor biasing?
4. Why base current is very small compared to emitter and collector current, when transistor is biased?
5. Why the transistor regions are doped with different impurities?
6. Name the three transistor configuration
7. Mention the different types of biasing circuits?.
8. What are the three regions of operation in a transistor?
9. What is Saturation region?
10. What is cut off region?
11. What is active region?
12. What is an amplifier? What are the types of Amplifiers?.
13. What is operating point or quiescent point?
14. What is voltage gain?
15. What is current gain?
16. What is coupling?
17. What are the different types of coupling?
18. Why it is called RC Coupled amplifier?
19. What type of biasing circuit is used in RC Coupled amplifier?
20. What is the function of coupling capacitor?
21. What is the function of voltage divider resistors?
22. What is the function of emitter resistor?
23. What is the function of the emitter bypass capacitor?
24. Define bandwidth?
25. What are the three parameters that cause the instability of transistor?
26. Define stability factor.
27. What is the phase of current and voltage at the output of the amplifier?
28. What about the current and voltage gain in CE amplifier?
29. Why CE configuration is widely used compared to CB configuration ?

OBSERVATION AND WORK SHEET

SEMILOG GRAPH SHEET HAS TO BE INSERTED

EXPERIMENT NO. 1(B)**RC COUPLED SINGLE STAGE FET AMPLIFIER****AIM**

To design RC coupled single stage FET amplifier and determine the gain, frequency response, input and output impedance.

COMPONENTS REQUIRED

Sl. No	Apparatus and components	Range	Quantity
1	Spring board		1
2	FET	BFW10/11	1
3	Resistors	2.7K Ω , 1K Ω , 2.2K Ω	1
4	Capacitors	0.1 μ F, 47 μ F	2+2
5	VRPS	0-30Vdc 3A	1
6	Signal generator	10Hz to 1MHz	1
7	CRO		1
8	Probes, wires		2+15
9	DRB	0 to 1Mohm	1
10	Digital Multimeter		2

THEORY

The field effect transistor (FET) has a capability to amplify a.c signals like a BJT. Depending upon the type of configuration, the FET amplifiers may be classified as:

- *Common source amplifier.
- *Common drain amplifier.
- *Common gate amplifier.

The circuit diagram 2.5 illustrates a common source junction FET amplifier. It is quite similar to a common emitter amplifier. Here, the resistors R_1 & R_2 are used to bias the FET. The coupling capacitors (C_{C1}, C_{C2}) are used to couple the a.c. input voltage source and the output voltage respectively, these are known as coupling capacitors. The capacitor C_s keeps the source of the FET efficiently at a.c. ground and is known as bypass capacitor.

The operation of the circuit may be understood from the assumption that when a small a.c. signal is made to apply to the gate, it produces variations in the gate to source voltage which in

turn, produces variations in the drain current. As the gate to source voltage increases, the drain current also increases because of this the voltage drop across the resistor R_D also increases. This causes the drain voltage to decrease. It means the positive half cycle of the output voltage produces the negative half cycle of the output voltage. In other words, there is a 180 degree phase shift between input and output amplifier. This phenomenon of phase inversion is similar to that exhibited by a common emitter bipolar transistor amplifier.

CIRCUIT DIAGRAM

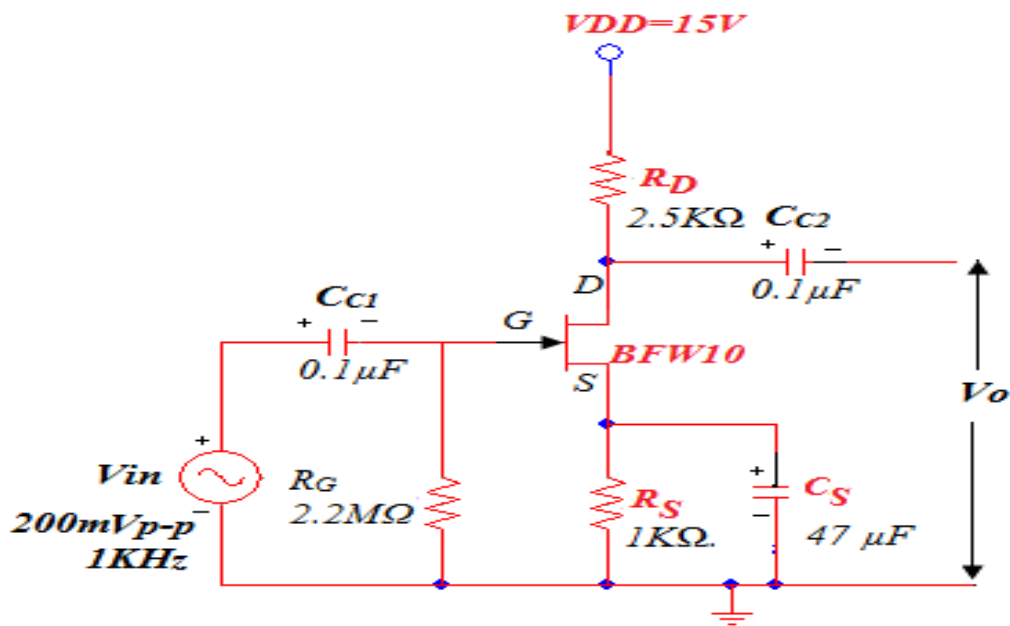


Fig 1(B).a Circuit to find the frequency response curve of FET amplifier

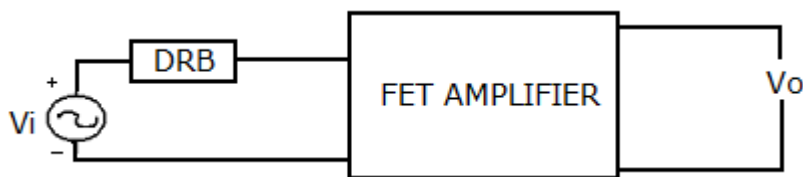


Fig 1(B).b Circuit to find the input impedance

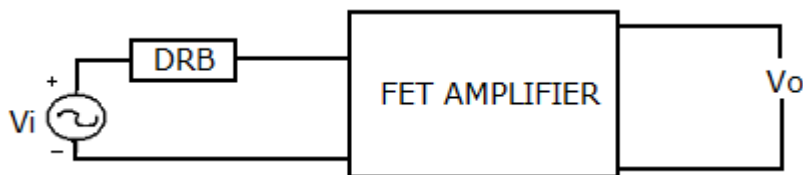


Fig 1(B).c Circuit to find the output impedance

DESIGN

Given: $I_{dss} = 8\text{mA}$; $V_p = -4\text{V}$; $g_m = 4\text{m mhos}$; $V_{DD} = +15\text{V}$;

Let $V_{GS} = -2\text{V}$;

$$I_d = I_{dss} (1 - V_{GS}/V_p)^2$$

$$= 2\text{mA}$$

$$V_s = I_d * R_s \text{ (Assume } I_d = I_s \text{)}$$

$$V_s = I_s * R_s$$

$$R_s = V_s / I_s = -V_{gs} / I_s = 2/2 = 1\text{K}\Omega.$$

Let $g_m = 4\text{m mhos}$

$$A_v = \mu = g_m * R_d$$

$$R_d = 10/4\text{m} = 2.5\text{K}\Omega \approx 2.7\text{K}\Omega$$

Let $C_{C1} = C_{C2} = 0.1\mu\text{F}$

$$C_s = 47\mu\text{F}$$

Input impedance is high hence select $R_G = 2.2\text{M}\Omega$

PROCEDURE

1. Rig up the circuit as shown in the circuit diagram and give $V_{DD} = +15\text{V}$ and without connecting signal generator check the biasing conditions i.e. V_{DS} , V_s and V_{GS} .
2. Connect the signal generator and set the input voltage constant (say 200mV) at 10KHz .
3. For different input frequencies note the corresponding output voltage.
4. Plot the frequency v/s decibel.
5. Find the figure of merit i.e. product of maximum gain and bandwidth.
6. Find the input and output impedance of the FET amplifier.
7. Connect the circuit as shown in Fig 2.b.
8. Set the DRB value to minimum initially and start increasing the resistance in the DRB from the minimum value until output voltage becomes half. When the output voltage becomes half of the initial value, the corresponding resistance in the DRB is the input impedance (Z_i).
9. Connect the circuit as shown in Fig 2.c.
10. Set the DRB value to maximum initially and start decreasing the resistance in the DRB from the maximum value until output voltage becomes half. When the output voltage becomes half of the initial value, the corresponding resistance in the DRB is the output impedance (Z_o).

--	--	--	--

Table 1(B).a To record the observed values

RESULT

The RC Coupled FET Amplifier was designed and the Bandwidth (BW), Input Resistance (Z_i), Output Resistance (Z_o) is

Bandwidth (BW) =

Input Resistance (Z_i) =

Output Resistance (Z_o) =

EXPECTED VIVA QUESTIONS

1. What happens to the gain when the amplifiers are connected in cascade?
2. What is field effect transistor?
3. Why FET is called unipolar device?
4. Differentiate between FET and BJT.
5. Mention the parameters of FET.
6. Define drain resistance (r_d).
7. Define Trans-conductance.
8. Define amplification factor.

OBSERVATION AND WORK SHEET

SEMILOG GRAPH SHEET HAS TO BE INSERTED

EXPERIMENT NO.2**BJT DARLINGTON EMITTER FOLLOWER****AIM**

To design BJT Darlington emitter follower with and without bootstrapping and determine the Voltage gain, input impedance and output impedance.

EQUIPMENTS REQUIRED:

Sl. No	Apparatus and components	Range	Quantity
1	Bread board		1
2	NPN transistor	SL100	2
3	Resistors	560 Ω , 480K Ω , 800K Ω	1 each
4	Capacitors	0.47 μ F, 47 μ F	2+2
5	VRPS	0-30V DC, 3A	1
6	Signal generator	10Hz to 3MHz	1
7	CRO for testing		1
8	Probes, wires		2+15
9	DRB	0 to 1M Ω	1
10	Digital multimeter		1

THEORY

A Darlington connection is a very popular connection of two transistors for operation as one super beta transistor. The composite transistor acts as a single unit with a current gain equal to the product of the current gains of individual transistors.

Sometimes, the current gain and input impedance of an emitter follower are insufficient to meet the requirement. In order to increase the overall values of circuit current gain and input impedance, two transistors are connected together. The result is that emitter current of the first transistor is the base current of the second transistor. Therefore the current gain of the pair is equal to product of individual current gain that is $\beta = \beta_1 * \beta_2$.

CIRCUIT DIAGRAM

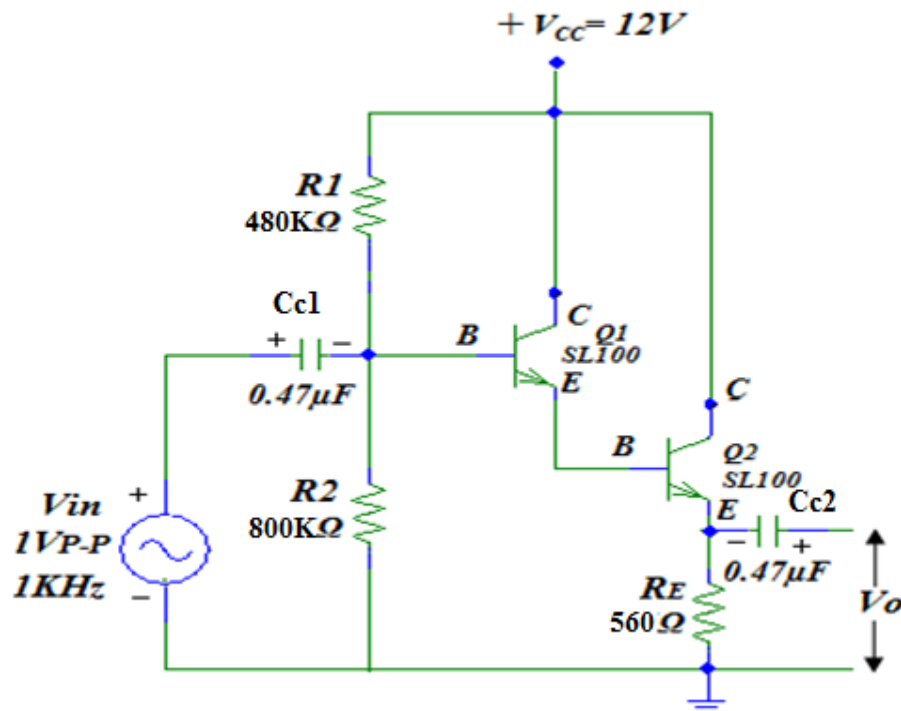


Fig 2.a Darlington emitter follower

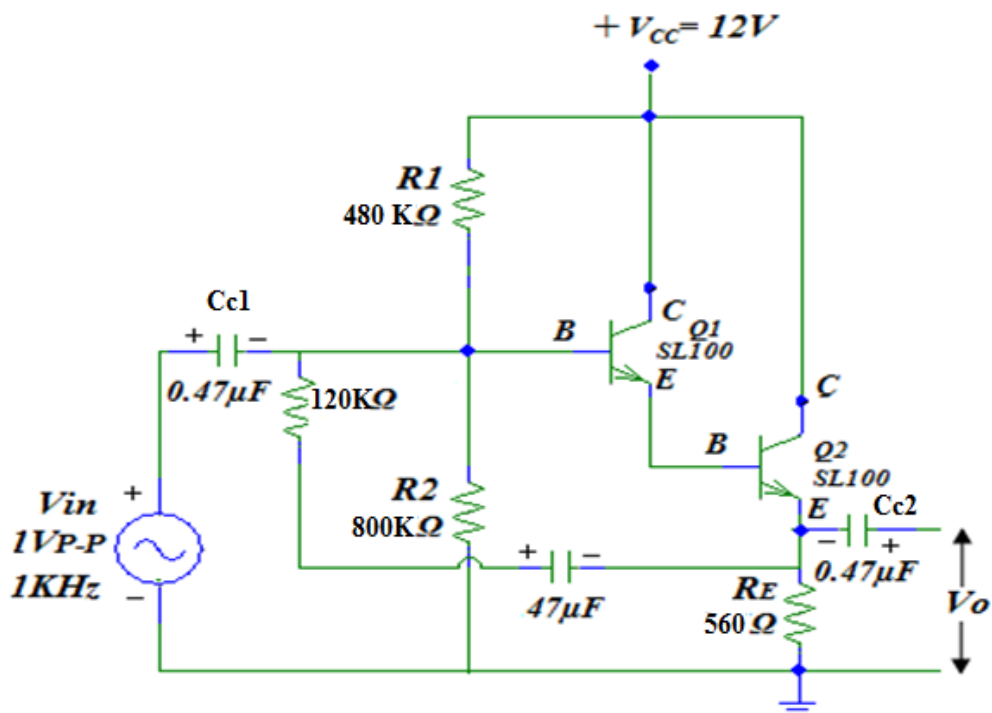


Fig 2.b Darlington emitter follower with bootstrapping

DESIGN

Let $V_{CE} = 6V$, $I_{CQ} \approx I_{EQ} = 10mA$ (Q point of transistor Q2), $\beta = 100$ (SL 100)

Then $V_{CC} = 2V_{CE} = 2 \times 6 = 12V$

$I_E = I_C = 10mA$

$V_{R3} = V_{CC} - V_{CE} = 12 - 6 = 6V$

$R_E = V_{R3} / I_E = 6V / (10mA) = 0.6K = 560\Omega$ (Choose)

$V_{R2} - V_{BE1} - V_{BE2} - V_{R3} = 0$

i.e, $V_{R2} = V_{BE1} + V_{BE2} + V_{R3}$
 $= 0.6 + 0.6 + (I_E R_E) = 1.2 + (10 \times 0.6) = 7.2V$

$V_{CC} = V_{R1} + V_{R2}$

$V_{R1} = V_{CC} - V_{R2} = 12 - 7.2 = 4.8V$

$I_{E1} = I_{B2} \approx I_{E2} / \beta = 10mA / 100 = 0.1mA$

$I_{B1} = I_{E1} / h_{fe} = 0.1mA / 100 = 1\mu A$

$R1 = V_{R1} / (10(I_{B1})) = 4.8 / (10 \times 1\mu A) = 480K\Omega$

$R2 = V_{R2} / (9I_{B1}) = 7.2 / (9 \times 1\mu A) = 800k\Omega$

To find Cc1

$X_{Cc1} \leq R_i / 10$ ($R_i = R1 \parallel R2 \parallel h_{ie} = h_{ie}$) Let $f_L = 100Hz$ (Lower Cut-off Frequency)

$f_L = 1 / (2\pi(R_i / 10)C_{c1})$

$R_i = R1 \parallel R2 \parallel h_{ie}$

For the above darlington pair $h_{ie} \approx \beta_D R_E$

For SL100 $\beta = 150$ and $\beta_D = \beta^* \beta = 22500$

$R_i \approx 290K\Omega$

So $C_{c1} = 1 / 2\pi(R_i/10)f_L = 1 / (2\pi \times 29K\Omega \times 100) = 0.05\mu F$

So, Use $C_{c1} = 0.1\mu F$ or $0.47\mu F$.

To find Cc2

Let $f_L = 100Hz$ (Lower Cut-off frequency), $R_L = 1K\Omega$

$f_L = 1 / 2\pi(R_o + R_L)C_E$

But $R_o = R_E \approx r_e$ Here, $r_e = V_T / I_C = 26mV / 10mA = 2.6\Omega$

$R_E \approx r_e \approx 3\Omega$

$1 / (2\pi f_L C_E) = R_E \Rightarrow$

Therefore, $C_E = 1 / (2\pi \times 100 \times (3 + 1K\Omega))$

$C_E = 1.59\mu F$

Use $C_{c2} \approx 0.47$ or $2\mu F$

PROCEDURE

Rig up the circuit as in the case of biasing circuit for RC coupled BJT Amplifier (Exp 1(A)) without connecting signal generator and capacitors. Check the biasing conditions i.e. $V_{CC} = 12V$ and check corresponding values of V_{CE} , V_{BE} , V_E .

1. Connect the as in Fig 2.a (without bootstrapping) with signal generator and designed capacitor values and set the input voltage constant at 50mV(p-p) , 1KHz.
2. Now vary the input frequency starting from 100Hz to MHz range and note the corresponding output voltage(peak to peak).
3. Plot the graph of frequency v/s output voltage gain in decibel with frequency on X-axis and dB gain on Y-axis and determine the bandwidth.
4. Repeat the procedure for circuit diagram in Fig 2.b (with bootstrapping)

TO DETERMINE INPUT IMPEDANCE (Z_i) AND OUTPUT IMPEDANCE (Z_o)

(a) INPUT IMPEADNCE (Z_i)

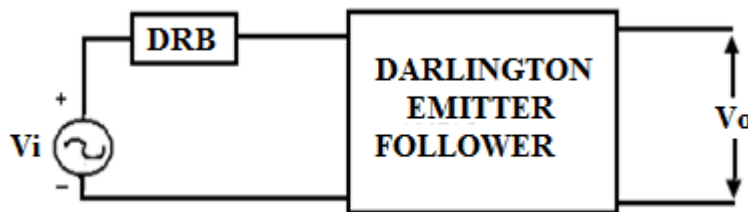


Fig 2.c Circuit to find the input impedance

PROCEDURE

1. Connect the circuit as shown in the Fig 2.c to obtain input impedance and set the input frequency at say 10kHz(center frequency).
2. Set the DRB value to minimum initially and note the corresponding output voltage. Start increasing the resistance in the DRB from the minimum value until output voltage becomes half. when the output voltage becomes half of the initial value, the corresponding resistance in the DRB is the input impedance(Z_i).
3. Repeat the procedure for circuit diagram in Fig 1.b (with bootstrapping)

(b) OUTPUT IMPEDANCE (Z_o)

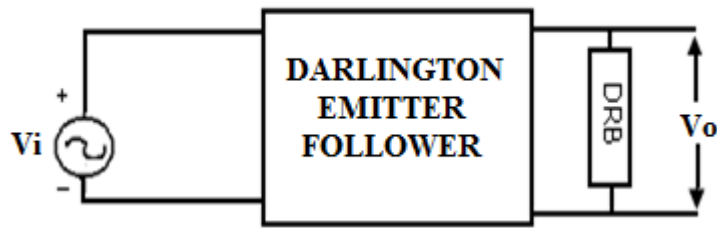


Fig 2.d - Circuit to find the output impedance

PROCEDURE

1. Connect the circuit as shown in the diagram 2.d to obtain output impedance and set the input frequency at say 10kHz(center frequency).
2. Set the DRB value to maximum initially and note the corresponding output voltage. Start decreasing the resistance in the DRB from the maximum value until output voltage becomes half. When the output voltage becomes half of the initial value, the corresponding resistance in the DRB is the output impedance (Z_o). Repeat the procedure for circuit diagram in Fig 1(A).b (with bootstrapping)
3. Repeat the procedure for circuit diagram in Fig 1.b (with bootstrapping)

EXPECTED GRAPH OF FREQUENCY RESPONSE

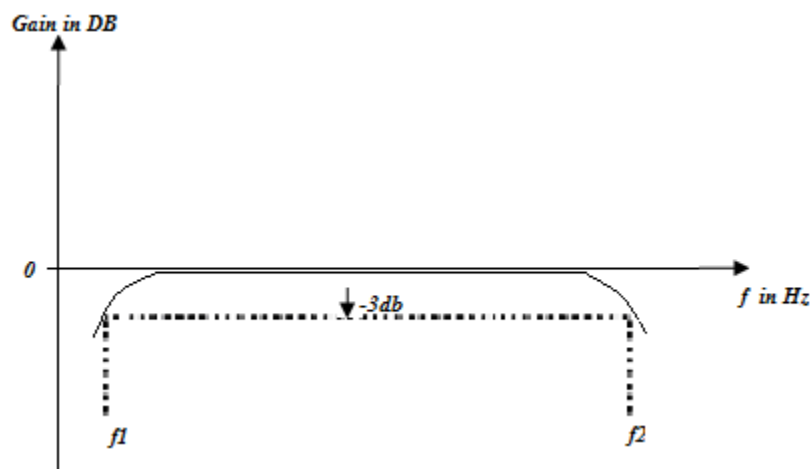


Fig 2.e Frequency response curve.

TABULAR COLUMN:

Frequency (Hz)	Output Voltage (V _{OP-P}) Volts	Voltage Gain V_o / V_i	Gain(dB) = $20 \log (V_o / V_i)$

Table 2.a. To record the observed values

RESULT

Midband Voltage Gain =

	With bootstrapping	Without bootstrapping
Input Resistance(Z_i)		
Output Resistance(Z_o)		

EXPECTED VIVA QUESTIONS

1. What is Darlington emitter follower?
2. Why do you call it as Darlington emitter follower?
3. What is the difference between with and without bootstrapping?
4. Benefits of with and without bootstrapping?
5. What is the difference between Darlington emitter follower and FET amplifier?
6. Mention the application of emitter follower?

OBSERVATION AND WORK SHEET

SEMILOG GRAPH SHEET HAS TO BE INSERTED

EXPERIMENT NO.4

RC PHASE SHIFT OSCILLATOR

AIM

To design and verify the performance of RC phase shift Oscillator for the given frequency.

EQUIPMENTS REQUIRED

Sl. No	Apparatus and components	Range	Quantity
01	Bread Board		1
02	NPN transistor	SL 100	1
03	Resistors	220 Ω , 5.6K Ω , 22K Ω , 820 Ω , 6.8K Ω	1+1+1+1+3
04	Capacitors	4.7 μ F, 0.001 μ F	2+3
05	VRPS	0-30Vdc 3A	1
06	Potentiometer	47k Ω	1
07	CRO for testing		1
08	Probes, wires		2+15
09	Digital multimeter		1

THEORY:

RC phase shift Oscillator basically consists of an amplifier and feed back network consisting of resistors and capacitors in ladder fashion. The basic RC circuit is as shown below

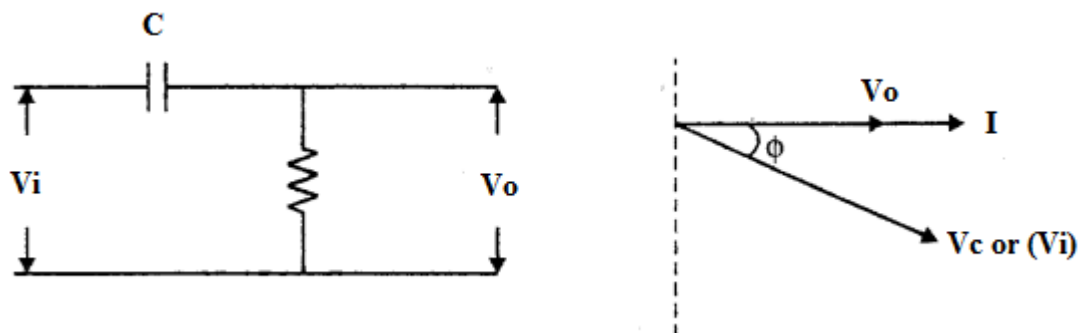


Fig 3.a Phase lead network and Phasor diagram

The current I is in phase with V_o , whereas the capacitor voltage V_c lags the current I by ϕ ($90^\circ \rightarrow$ Ideal value).

OR the output voltage V_o leads the I/P voltage V_i by angle ϕ is adjusted in practice, equal to 60° . RC network is used in feedback path. In Oscillator, feedback network must introduce a phase shift of

180° to obtain total phase shift around a loop as 360°. Thus three RC network each provide 60° phase shift is cascaded, so that it produces total 180° phase shift. The Oscillator circuit consisting amplifier and RC feedback network is as shown below.

CIRCUIT DIAGRAM:

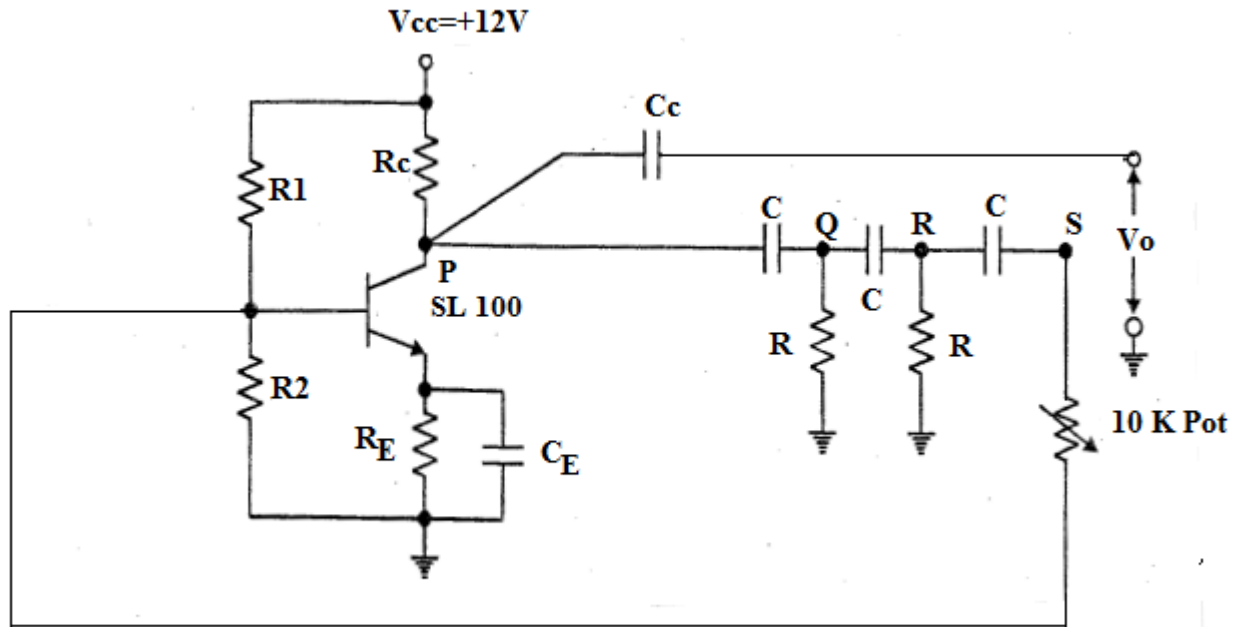


Fig 3.b Circuit diagram of Phase Shift Oscillator

DESIGN

AMPLIFIER CIRCUIT DESIGN

Let $V_{CC} = 12\text{ V}$, $I_C = 4\text{ mA}$, $h_{fe} = \beta = 100$

Let $V_E = 2\text{ V}$, $V_{CE} = V_{CC} / 2 = 6\text{ V}$

$$\therefore R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C} = \frac{2}{4\text{ mA}} = 0.5\text{ K}\Omega = 500\text{ }\Omega$$

Use $R_E = 470\text{ }\Omega$

To Find R_C :

Applying KVL to CE loop

$$V_{CC} - I_C * R_C - V_{ce} - V_e = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{12 - 6 - 2}{4\text{ mA}} = 1\text{ K}\Omega$$

Use $R_c = 1 \text{ K}\Omega$

From the biasing circuit in the above figure,

We can assume $V_B = V_{CC} \frac{R_2}{R_1 + R_2}$ since I_B is negligible

We know $V_B = V_{BE} + V_E = 2 + 0.7 = 2.7 \text{ V}$

$$\begin{aligned}\therefore \frac{V_B}{V_{CC}} &= \frac{R_2}{R_1 + R_2} \\ \frac{2.7}{12} &= \frac{R_2}{R_1 + R_2} \\ 0.225 &= \frac{R_2}{R_1 + R_2}\end{aligned}$$

$$0.225 R_1 + 0.225 R_2 = R_2$$

$$0.225 R_1 = 0.775 R_2$$

$$R_1 = 3.44 R_2$$

Say if $R_2 = 6.8 \text{ K}\Omega$

then $R_1 = 23.3 \text{ K}\Omega$, **Use $R_1 = 22 \text{ K}\Omega$**

To Design C_E

Let $X_C = R_E / 10$, at $f_L = 100 \text{ Hz}$

$$1 / (2\pi f C_E) = R_E / 10 = 470 \Omega / 10$$

Therefore

$$C_E = 1 / (2\pi \cdot 100 \cdot 47) = 33.8 \mu\text{F}$$

Use $C_E = 47 \mu\text{F}$

To design C_c

$$f_L = 1 / (2\pi (R_o + R_L) C_c)$$

For the above circuit $R_o = R_c = 1 \text{ K}\Omega$ and let $R_L = 1 \text{ K}\Omega$

$$\text{So } C_c = 1 / (2\pi \cdot 2 \text{ K}\Omega \cdot 100) = 0.79 \mu\text{F}$$

Use $C_c = 0.47 \mu\text{F}$ (ceramic)

DESIGN OF PHASE-SHIFTING NETWORK

The frequency of Oscillations is determined by phase shifting network. The Oscillating frequency for the above circuit is given by

$$f = \frac{1}{2\pi RC \sqrt{6+4K}}$$

where $K = \frac{R_C}{R}$ which is usually < 1

Let $f = 2 \text{ KHz}$ (Audio frequency range 20 Hz to 20 KHz)

and $R = 2.2 \text{ K}\Omega$

$$\therefore K = \frac{R_C}{R} = \frac{1 \text{ K}}{2.2 \text{ K}} = 0.454$$

$$\therefore f = \frac{1}{2\pi RC \sqrt{6 + 4(0.454)}}$$

$C = 0.0129 \text{ }\mu\text{F}$

Use $C = 0.01 \text{ }\mu\text{F}$

Note :

- The last Resistor in the phase shifting network is chosen to be a 10 K pot. This is done to get a overall phase shift of 180° at frequency of Oscillations.
- The minimum h_{fc} required for the transistor to Oscillate is

$$h_{fe \text{ min}} = 23 + 29 \cdot \frac{R}{R_C} + 4 \cdot \frac{R_C}{R}$$

Where $R_C = 1 \text{ K}\Omega$ and $R = 2.2 \text{ K}\Omega$ (Phase shifting network)

$$\therefore h_{fe \text{ min}} = 23 + 29 \cdot \frac{2.2 \text{ K}}{1 \text{ K}} + 4 = \frac{1 \text{ K}}{2.2 \text{ K}} = 89$$

The transistor should be chosen to have a value of h_{fe} greater than 89.

$$0.225 R_1 + 0.225 R_2 = R_2$$

$$0.225 R_1 = 0.775 R_2$$

$$R_1 = 3.44 R_2$$

Say if $R_2 = 6.8 \text{ K}\Omega$

then $R_1 = 23.3 \text{ K}\Omega$, Choose $R_1 = 22 \text{ K}\Omega$

Using Coupling Capacitor $C_C = 0.47 \text{ }\mu\text{f}$

$$C_B = 50 \text{ }\mu\text{f} \cong 47 \text{ }\mu\text{f}$$

PROCEDURE:

- ❖ Make the circuit connections as shown in Fig 3.b
- ❖ The output V_o is obtained on CRO. The $10 \text{ K}\Omega$ pot is adjusted to get a stable output on the CRO.
- ❖ The frequency of Oscillations is measured using CRO and then compared with the theoretical values.
- ❖ With respect to output at point P, the waveforms at point Q, R and S are observed on the CRO. We can see the phase shift at each point being 60° , 120° and 180° respectively.

NOTE:

The value of all three capacitors C is changed and the frequency of Oscillation can be changed to new value and is measured again.

Designed frequency 2 KHZ

Actual frequency got 2KHZ

Phase shift between	P & Q	60
	P & R	120
	P & S	180

RESULTS :

Theoretical frequency of oscillations = KHz

Practical frequency of oscillations = KHz

EXPERIMENT NO. 4(A)

BJT HARTELY OSCILLATOR

AIM

To Design Hartley oscillator using BJT for the given frequency 100 kHz.

COMPONENTS REQUIRED

Sl. No	Apparatus and components	Range	Quantity
01	Bread board		1
02	NPN transistor	SL100	1
03	Resistors	470 Ω , 1K Ω , 22K Ω , 6.8K Ω	1
04	Capacitors	10 μ F, 0.1 μ F, 0.001 μ F	1+2+1
05	VRPS	0-30V DC, 3A	1
06	CRO for testing		1
07	Probes, wires		1
08	Multimeter for testing		1
09	Potentiometer	10 K Ω	1

THEORY

HARTLEY OSCILLATOR:

If the oscillator uses two inductors and one capacitor in the feedback (or Tank) circuit, then it is called as Hartley oscillator.

The Hartley oscillator is quite popular oscillator is widely used as local oscillator in the radio receivers. The circuit diagram 5.1.a consists of single stage of an RC coupled amplifier. The resistance R_1 , R_2 and R_E form the biasing and stabilization network. The emitter bypass capacitor offers low reactance path to the signal, without it, the voltage gain of each stage would be lost. The coupling capacitors at the input and output of transistor transmits A.C. signal but blocks D.C. .This prevents D.C. interference between various stages and the shifting of operating point. And LC tank circuit.

The tank circuit consists of two series inductors L_1 and L_2 forming potential divider used to provide the feedback voltage. The voltage developed across L_1 and L_2 provides regenerative feedback needed for sustained oscillations. Transistor itself produces a phase shift of 180° and another addition

phase shift of 180° is provided by inductive feedback. This means that a total phase shift of 360° is obtained satisfying the conditions required for developing oscillations.

CIRCUIT DIAGRAM

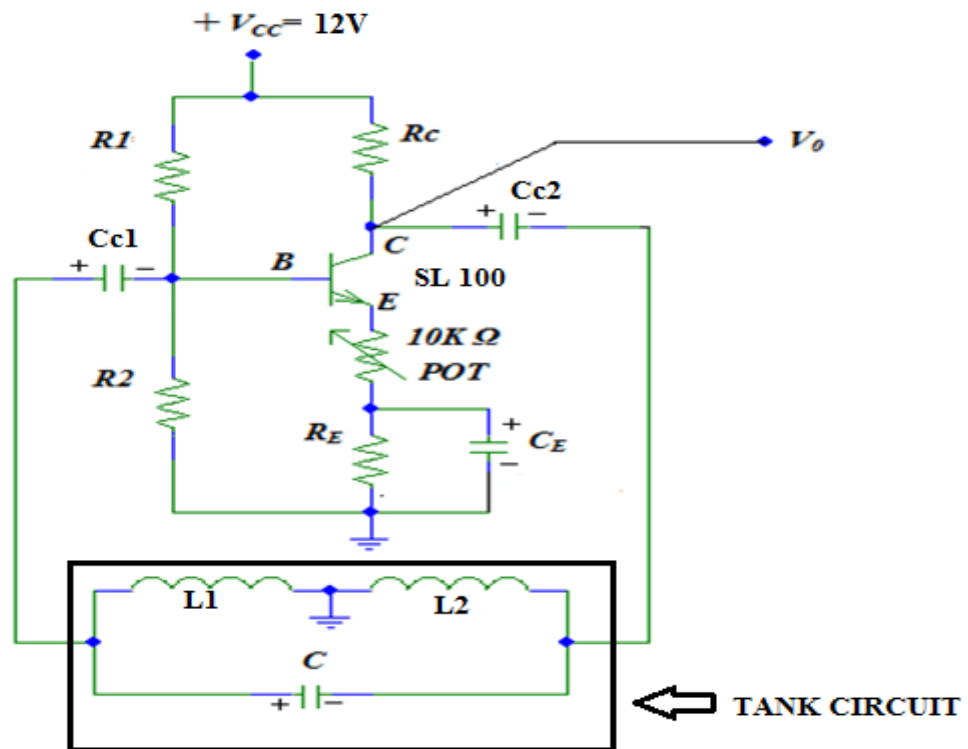


Fig 4(A).a Hartley oscillator

DESIGN OF AMPLIFIER CIRCUIT

Let $V_{CC}=12\text{ V}$, $I_C=4\text{ mA}$, $\beta=100$ (for SL 100)

As usual we can assume $V_{RE} = V_E = V_{CC}/10 = 10/10 = 1.2\text{ V}$

To find R_E :

$$V_E = I_E R_E = 1.2\text{ V}$$

$$R_E = V_E / I_E$$

$$= V_E / I_C \text{ (as } I_E \approx I_C \text{)}$$

$$= 1.2\text{ V} / 4\text{ mA}$$

$$= 500\Omega$$

use $R_E = 470\Omega$ (standard) in series with $1\text{ K}\Omega$ pot (to provide gain control)

To find R_C:

Let $V_{CE} = V_{CC}/2$ (Q point in middle of active region)
 $= 12/2 = 6V$

Apply KVL in CE loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$12 - (4m * R_C) - 5 - 1 = 0$$

$$R_C = 1K\Omega$$

To find R₁ & R₂:

Let a current of $10I_B$ flows through R_1 and $9I_B$ flows through R_2

$$V_B = V_{BE} + V_{RE}$$

$$V_B = 0.7 + 1.2 = 1.9V$$

$$I_C = \beta I_B$$

$$I_B = I_C / \beta = 4m / 100 = 40\mu A$$

$$R_1 = (V_{CC} - V_B) / (10 I_B) = (12 - 1.9) / (40 * 10^{-6} * 10) = 23 K\Omega \quad \text{Use } R_1 = 22K\Omega$$

$$R_2 = V_B / (9 I_B) = 2.7 / (9 * 40 * 10^{-6}) = 7.5K\Omega \quad \text{Use } R_2 = 6.8K\Omega$$

To design C_E

Let $f_L = 500Hz$ (Lower Cut-off frequency)

$$f_L = 1 / (2\pi * R_E * C_E)$$

But $R_E \approx r_e$ Here $r_e = V_T / I_C = 26mV / 4mA = 6.5\Omega$

$$R_E \approx r_e \approx 6.5\Omega$$

$$1 / (2\pi * f_L * C_E) = R_E \Rightarrow$$

Therefore, $C_E = 1 / (2\pi * 500 * 6.5)$

$$C_E = 49 \mu F$$

Use $C_E \approx 50 \mu F$ or $10 \mu F$

To design C_{c1}

$$f_L = 1 / (2\pi * (R_i / 10) * C_{c1})$$

$$R_i = R_1 \parallel R_2 \parallel h_{ie} \quad \text{Where } h_{ie} = \beta * r_e$$

For SL100 $\beta = 150$ and $r_e = 6.5\Omega$, $h_{ie} = 150 * 6.5 \approx 1K\Omega$

$$R_i \approx h_{ie} = 1K\Omega$$

$$\text{So } C_{c1} = 1 / (2\pi * R_i * f_L) = 1 / (2\pi * (1K\Omega / 10) * 500) = 3.18 \mu F$$

Use $C_{c1} = 3 \mu F$ or $0.47 \mu F$.

To design Cc2

Let $R_L = 1K\Omega$

$$f_L = 1 / (2\pi * ((R_o + R_L)/10) * C_{c2})$$

For the above circuit $R_o = R_c = 1K\Omega$ and let $R_L = 1K\Omega$

$$\text{So } C_{c2} = 1 / (2\pi * 0.2K\Omega * 500) = 1.59 \mu F$$

Use $C_{c1} = C_{c2} = 2 \mu F$ or $0.47 \mu F$ (ceramic)

TANK CIRCUIT DESIGN

Given $f = 100KHz$

$$f = 1 / 2\pi \sqrt{L_{eq} C}$$

Let $L_{eq} = L_1 + L_2 = 2mH$ Use $L_1 = L_2 = 1mH$

$$C = 1 / (4\pi^2 * 2mH * f^2)$$

$$C = 0.0012 \mu F$$

Use $C = 0.001 \mu F$

PROCEDURE

1. Rig up the circuit diagram as shown in the circuit diagram without the tank circuit and check the biasing conditions with $V_{cc} = 12V$ i.e. check V_{CE} , V_{BE} and V_E .
2. Connect the tank circuit and vary the 10K pot to get proper sine wave across the output terminals and check the frequency of output waveform and compare it with the theoretical value and tabulate the readings.

EXPECTED OUTPUT WAVEFORM

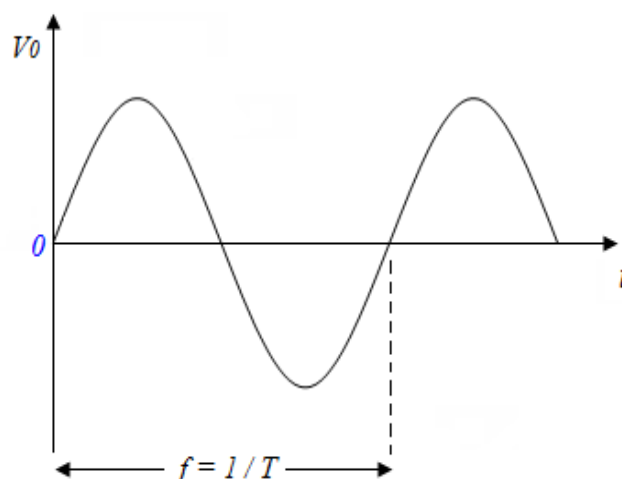


Fig 4(A).b Output Waveform for Hartley oscillator

TABULAR COLUMN

HARTLEY OSCILLATOR

$L_1(\text{mH})$	$L_2(\text{mH})$	$L_{eq}(\text{mH})$	$C(\mu\text{F})$	$f_{th}(\text{Hz})$	$f_{prac}(\text{Hz})$

Table 4(A).a To record the experimental values of Hartley circuit

RESULT

Hartley's Oscillator: f_0 (observed) = _____Hz

f_0 (designed) = _____Hz

OBSERVATION AND WORK SHEET

EXPERIMENT NO. 4(B)

BJT COLPITTS OSCILLATOR

AIM

To design Colpitts oscillator using BJT for the given frequency 100 kHz.

COMPONENTS REQUIRED

Sl. No	Apparatus and components	Range	Quantity
01	Bread board		1
02	NPN transistor	SL 100	1
03	Resistors	470 Ω , 1K Ω , 22K Ω , 6.8K Ω	1
04	Capacitors	10 μ F, 0.1 μ F, 0.001 μ F, 0.002 μ F	1+2+1+1
05	VRPS	0-30V DC, 3A	1
06	CRO for testing		1
07	Probes, wires		1
08	Multimeter for testing		1
09	Potentiometer	10K Ω	1

THEORY

COLPITTS OSCILLATOR:

If the oscillator uses two capacitors and one inductor in the feedback(or Tank) circuit, then it is called as colpitts oscillator.

The working principle of Hartley and colpitts oscillators is same, only difference is that the tank circuit is designed with two capacitors and one inductor for providing oscillations. The function of all the components present in the colpitts oscillator circuit is same as Hartley oscillator.

CIRCUIT DIAGRAM

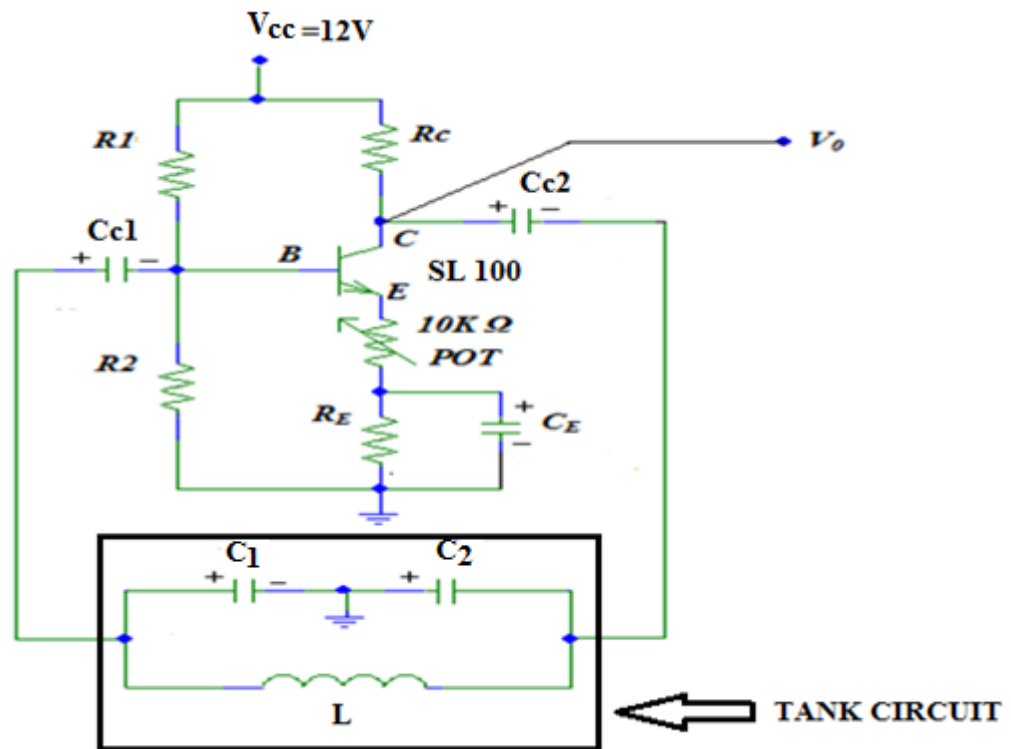


Fig 4(B).a Colpitts oscillator

DESIGN OF AMPLIFIER CIRCUIT

Let $V_{CC}=12\text{ V}$, $I_C=4\text{ mA}$, $\beta=100$ (for SL 100)

As usual we can assume $V_{RE} = V_E = V_{CC}/10 = 12/10 = 1.2\text{ V}$

To find R_E :

$$V_E = I_E R_E = 1.2\text{ V}$$

$$R_E = V_E / I_E$$

$$= V_E / I_C \text{ (as } I_E \approx I_C \text{)}$$

$$= 1.2\text{ V} / 4\text{ mA} = 300\Omega$$

Use $R_E = 470\Omega$ (standard) in series with $1\text{ K}\Omega$ pot (to provide gain control)

To find R_C :

Let $V_{CE} = V_{CC}/2$ (Q point in middle of active region)

$$= 12/2 = 6\text{ V}$$

Apply KVL in CE loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$12 - (4\text{ mA} \cdot R_C) - 6 - 1 = 0$$

$$R_C = 1\text{ K}\Omega$$

To find R1 & R2:

Let a current of $10I_B$ flows through R_1 and $9I_B$ flows through R_2

$$V_B = V_{BE} + V_{RE}$$

$$V_B = 0.7 + 1.2 = 1.9V$$

$$I_C = \beta I_B$$

$$I_B = I_C / \beta = 4m / 100 = 40\mu A$$

$$R_1 = (V_{CC} - V_B) / 10 I_B = (12 - 1.9) / (40 \times 10^{-6} \times 10) = 23 K\Omega \quad \text{Use } R_1 = 22K\Omega$$

$$R_2 = V_B / 9 I_B = 2.7 / (9 \times 40 \times 10^{-6}) = 7.5 K\Omega \quad \text{Use } R_2 = 6.8 K\Omega$$

To find C_E

Let $f_L = 500Hz$ (Lower Cut-off frequency)

$$f_L = 1 / 2\pi R_E C_E$$

But $R_E \approx r_e$ Here $r_e = V_T / I_C = 26mV / 4mA = 6.5\Omega$

$$R_E \approx r_e \approx 6.5\Omega$$

$$1 / (2\pi f_L C_E) = R_E \Rightarrow$$

Therefore, $C_E = 1 / (2\pi \times 500 \times 6.5)$

$$C_E = 49 \mu F$$

Use $C_E \approx 50 \mu F$ or $10 \mu F$

To find C_{c1} and C_{c2}

Assume $C_{c1} = C_{c2} = 0.47\mu F$ (ceramic) (Design same as Hartley Oscillator)

TANK CIRCUIT DESIGN

Given $f = 100KHz$

$$f = 1 / 2\pi \sqrt{L C_{eq}}$$

Let $C_1 = 0.001\mu F$; $C_2 = 0.002\mu F$

$$C_{eq} = (C_1 \times C_2) / (C_1 + C_2) = 0.666nF$$

$$L = 1 / (4\pi^2 \times 0.66nF \times f^2) \approx 0.0038H$$

Use $L \approx 3.8mH$

PROCEDURE

1. Rig up the circuit diagram as shown in the circuit diagram without the tank circuit and check the biasing conditions with $V_{CC} = 12V$ i.e. check V_{CE} , V_{BE} and V_E .
2. Connect the tank circuit and vary the 10K pot to get proper sine wave across the output terminals and check the frequency of output waveform and compare it with the theoretical value and tabulate the readings.

EXPECTED OUTPUT WAVEFORM

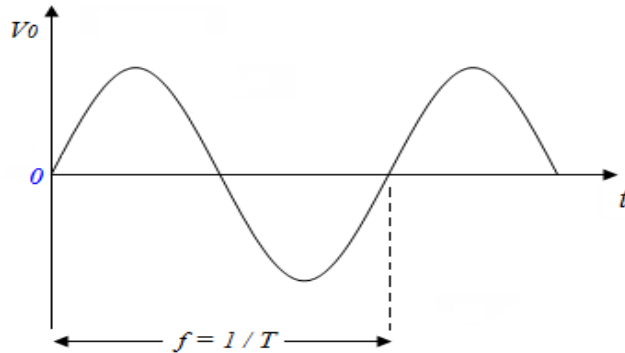


Fig 4(B).b Output Waveform for Hartley oscillator

TABULAR COLUMN

$C_1(\mu\text{f})$	$C_2(\mu\text{f})$	$C_{eq}(\mu\text{F})$	$L(\text{mH})$	$f_{th}(\text{Hz})$	$f_{prac}(\text{Hz})$

Table 4(B).a To record the experimental values of Colpitt's circuit

RESULT

Colpitt's Oscillator: f_0 (observed) = _____ Hz

f_0 (designed) = _____ Hz

EXPECTED VIVA QUESTIONS

1. What is feed back?
2. What is Negative feedback?
3. What is positive feedback (regenerative feedback)?
4. What is Barkhausen criterion?
5. What is an oscillator?
6. What type of feedback is used in oscillator?
7. What type of feedback is used in amplifier?
8. Mention the mainly used feedback networks in oscillators.
9. Give the examples for high frequency oscillator?
10. Give the examples for low frequency oscillators?
11. Define Hartley oscillators.
12. Define Colpitts oscillators.
13. What are the differences between colpitts oscillator and Hartley oscillators?

EXPERIMENT NO.5**BJT CRYSTAL OSCILLATOR****AIM**

To design and test BJT Crystal oscillator for the given frequency.

COMPONENTS REQUIRED

SL. NO	APPARATURS AND COMPONENTS	RANGE	QUANTITY
01	Bread Board		1
02	NPN transistor	SL100	1
03	Resistors	470 Ω , 1K Ω , 22K Ω , 6.8K Ω	3
04	Capacitors	0.01 μ F , 0.1 μ F	2+1
05	VRPS	0-30V DC, 3A	1
06	CRO for testing		1
07	Probes, wires		1+15
08	Crystal	2M Hz	1
09	Signal generator	10Hz to 3MHz	1

THEORY

Crystal oscillators are made from quartz. A crystal can be operated in the series resonant or parallel resonant mode. In the series mode crystal offers minimum impedance at resonance and in parallel mode it offers maximum impedance and is inductive. Since the parallel resonant frequency of a crystal is slightly higher than its series resonant frequency, the method of connection is important. In this experiment we will construct oscillators by connecting the crystal in the parallel resonant mode. But both oscillator's exhibit good stability, but the sine wave outputs may be slightly distorted. In transistor crystal oscillator, note that it is a colpitt's oscillator modified to acts as a crystal oscillator the only change in the addition of the crystal in the feedback network. The crystal will act as a parallel tuned circuit, as you can see in this circuit 6.6 that instead of resonance caused by L and C. We have the parallel resonance of the crystal at parallel resonance the impedance of the crystal is maximum this means that there is a maximum voltage drops across crystal this in turn will allow the maximum energy through the transistor feedback network at resonance frequency. We note that feedback is positive and phase shift in 180° is produced by the transistor a further phase shift of 180° is produced by the capacitor voltage divider this oscillator will oscillate only at resonance frequency even the

smallest deviation from resonance frequency will cause the oscillator to act as an ineffective short consequently we have an extremely stable oscillator.

Advantages:

1. They have an order of frequency stability.
2. The quality factor of the crystal is very high.

Disadvantages:

1. They are fragile and consequently can only be used in low power circuit.
2. The frequency of oscillations cannot be changed appreciably.

CIRCUIT DIAGRAM

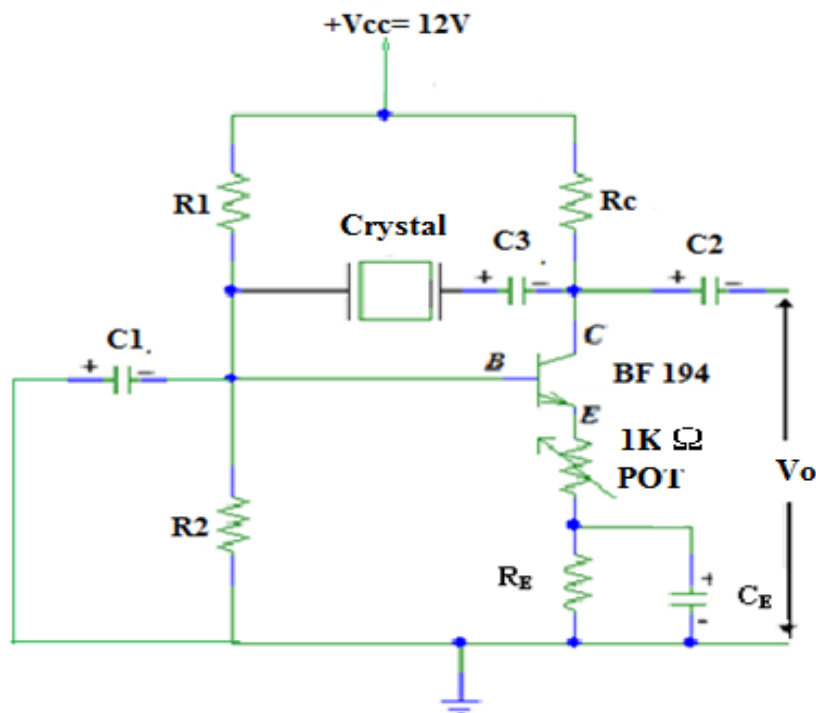


Fig 5.a – Crystal oscillator

DESIGN OF AMPLIFIER CIRCUIT

Let $V_{CC}=12\text{ V}$, $I_C=4\text{ mA}$, $\beta=100$ (for SL 100)

As usual we can assume $V_{RE} = V_E = V_{CC}/10 = 10/10 = 1.2\text{ V}$

To find R_E :

$$V_E = I_E R_E = 1.2\text{ V}$$

$$R_E = V_E / I_E$$

$$= V_E / I_C \text{ (as } I_E \approx I_C \text{)}$$

$$= 1.2\text{ V} / 4\text{ mA} = 500\Omega$$

Use $R_E = 470\Omega$ (standard) in series with $1\text{ K}\Omega$ pot (to provide gain control)

To find R_C:

Let $V_{CE} = V_{CC}/2$ (Q point in middle of active region)
 $= 12/2 = 6V$

Apply KVL in CE loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$12 - (4m * R_C) - 5 - 1 = 0$$

$$R_C = 1K\Omega$$

To find R₁ & R₂:

Let a current of $10I_B$ flows through R_1 and $9I_B$ flows through R_2

$$V_B = V_{BE} + V_{RE}$$

$$V_B = 0.7 + 1.2 = 1.9V$$

$$I_C = \beta I_B$$

$$I_B = I_C / \beta = 4m / 100 = 40\mu A$$

$$R_1 = (V_{CC} - V_B) / (10I_B) = (12 - 1.9) / (40 * 10^{-6} * 10) = 23 K\Omega \quad \text{Use } R_1 = 22K\Omega$$

$$R_2 = V_B / (9I_B) = 2.7 / (9 * 40 * 10^{-6}) = 7.5K\Omega \quad \text{Use } R_2 = 6.8K\Omega$$

To find C_E

Let $f_L = 500Hz$ (Lower Cut-off frequency)

$$f_L = 1 / (2\pi * R_E * C_E)$$

$$\text{But } R_E \approx r_e \quad \text{Here } r_e = V_T / I_C = 26mV / 4mA = 6.5\Omega$$

$$R_E \approx r_e \approx 6.5\Omega$$

$$1 / (2\pi * f_L * C_E) = R_E \Rightarrow$$

$$\text{Therefore, } C_E = 1 / (2\pi * 500 * 6.5)$$

$$C_E = 49 \mu F$$

$$\text{Use } C_E \approx 50 \mu F \text{ or } 10 \mu F$$

Use C_1 and C_2 0.01 uF each and $C_3 = 0.1 uF$.

PROCEDURE

1. Rig up the circuit as shown in the circuit diagram without the crystal and check the biasing conditions i.e. $V_{CC} = 12V$ and check V_{CE} , V_{BE} , V_E .
2. Connect the crystal and vary the 1K(or 10K) pot to get proper sine wave across the output terminals and check the frequency of output waveform and compare it with the theoretical value and tabulate the readings

EXPECTED OUTPUT WAVEFORMS

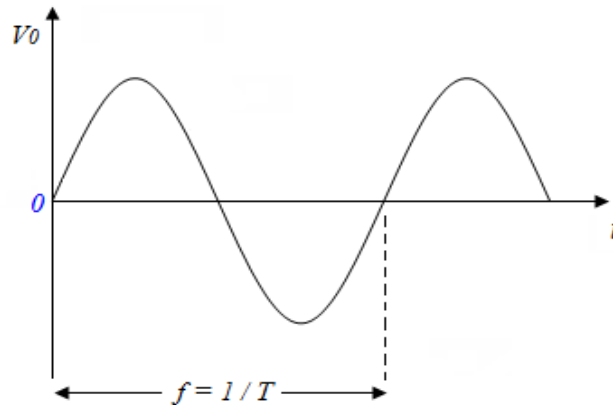


Fig 5.b – Output waveform of Crystal oscillators

RESULT

1. The Theoretical frequency of the given crystal is _____MHz
2. The frequency of the output waveform obtained practically is_____MHz.

EXPECTED VIVA QUESTIONS

1. Define crystal oscillator
2. What type of crystal is used and why?
3. What is the difference between crystal oscillator and other types of oscillators?.
4. What do you mean by feedback?
5. What is Negative feedback?
6. What is positive feedback (regenerative feedback)?
7. What is Barkhausen criterion?
8. What is an oscillator?
9. What type of feedback is used in oscillator?
10. What type of feedback is used in an amplifier?
11. Mention the mainly used feedback networks in oscillators.
12. Give the examples for high frequency oscillator?
13. Give the examples for low frequency oscillators?

OBSERVATION AND WORK SHEET

EXPERIMENT NO.6**DIODE CLIPPING CIRCUITS****AIM**

To design and Verify Diode clipping circuits (single and double ended) for peak detection and peak clipping.

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Resistors	10K Ω	1
04	VRPS	0-30V DC, 3A	1
05	CRO for testing		1
06	Signal generator	10Hz to 1MHz	1
07	Probes, wires		1
08	Digital multimeter		1

THEORY

Clippers are networks that employ diodes to clip away portions of an input signal without distorting the remaining part of the applied signal. These clipper circuits transfer a selected portion of the input waveform to the output. Diode clipping circuits are used to prevent a waveform from exceeding some particular limit in either negative or positive or both sides of it . This is achieved by connecting the diode in serial or in parallel circuit. Variable DC voltage is connected in the circuit to achieve required level of clipping. By using different levels of DC voltages, it is possible to get different level of clipping in positive and negative side. The circuit with which the waveform is shaped by removing a portion of the applied wave is known as a clipping circuit.

Clipping circuits are used to select and transmitting that part of an arbitrary waveform which lies above or below some reference level. Clipping circuit, also referred to as voltage limiters, amplitude selectors or slicers. A clipping circuit comprises of linear elements like resistors and non linear elements like junction diode or transistor, but do not contain energy storage elements like capacitors. Clippers find extensive use in radar, digital and other electronics systems. These clipper circuits are also called as limiters.

Following are few types of clipper circuits

1. Single ended (positive or negative) and double ended clipping
2. Series or parallel based on the construction.

There are generally two categories of clippers: **series** and **parallel** to load. In series configuration diode is in series with the load, but in parallel the diode is parallel to load.

Peak detection is possible by connecting a suitable capacitor across the output of single ended clipping circuit. The capacitor charging time to be fast and discharging time to be slow so that capacitor holds the maximum value.

6(A) SHUNT CLIPPERS (SINGLE ENDED CLIPPING)

6(A).1 CLIPPING ABOVE THE REFERENCE VOLTAGE(V_{ref})

CIRCUIT DIAGRAM

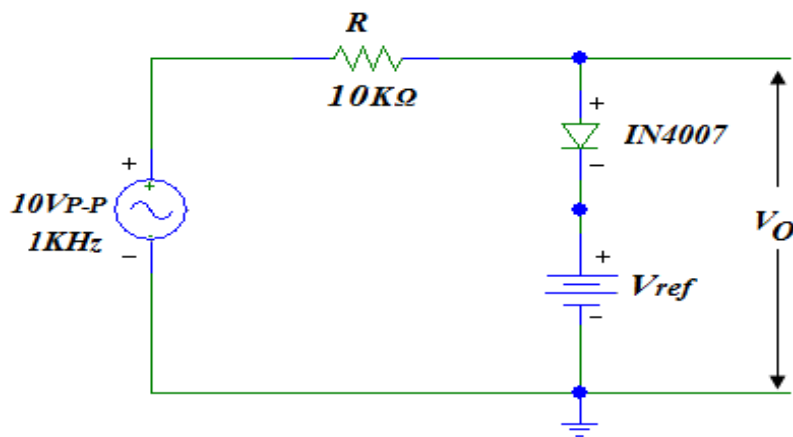


Fig 6(A).1.a Shunt clipper for clipping above the reference level.

DESIGN

Let the output voltage be clipped at say $V_o = +4V$

Therefore $V_o(\max) = +4V$

From Fig 7(B).1.a above, $V_o(\max) = V_f + V_{ref}$ (Where $V_f = V_K =$ cut in voltage of the diode $\approx 0.6V$)

Therefore $V_{ref} = V_o(\max) - V_f = 4 - 0.6 = 3.4V$

The value of resistor R is designed usually by equation $R = \sqrt{R_f R_r}$

Where $R_f =$ diode forward resistance $= 10\Omega$

and $R_r =$ diode reverse resistance $= 10M\Omega$

Therefore $R = \sqrt{10 \times 10 \times 10^6} = 10K\Omega$

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(A).1.a
2. Switch on the VRPS and set the supply voltage $V_{ref}=3.4V$
3. Apply a Sine Wave input (V_{in}) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply V_{in} and V_o to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

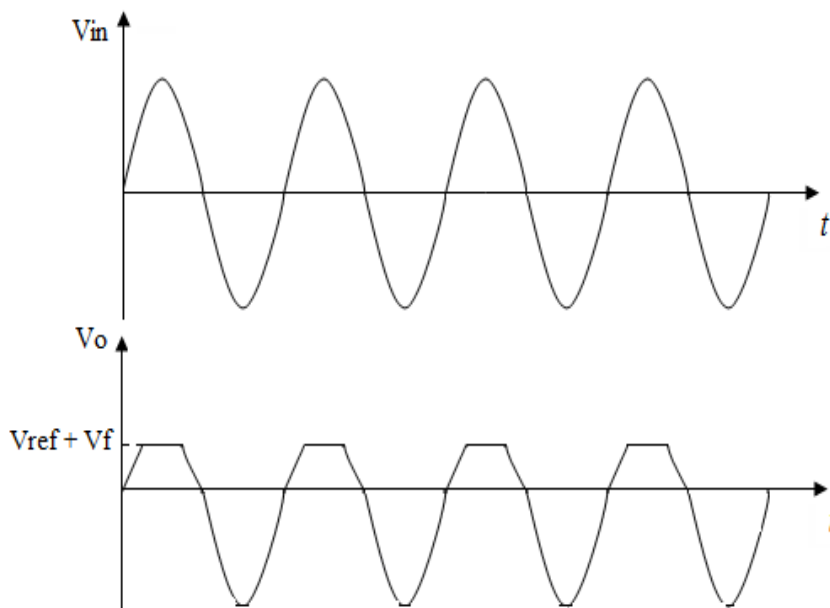
OUTPUT WAVEFORM

Fig 6(A).1.b Wave form of shunt clipper for clipping above reference level.

TRANSFER CHARACTERISTICS

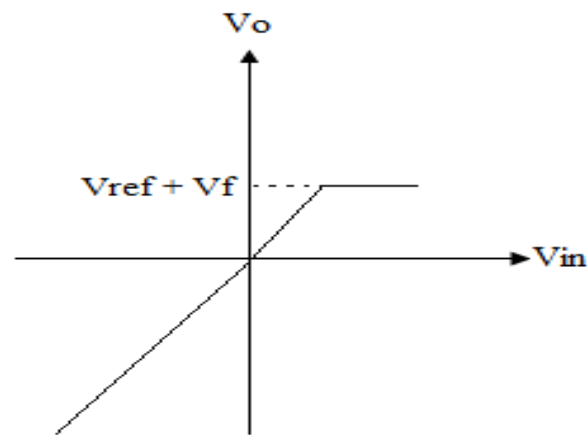


Fig 6(A).1.c Transfer characteristics of shunt clipper for clipping above reference level.

6(A).2 CLIPPING BELOW THE REFERENCE VOLTAGE(V_{ref})

CIRCUIT DIAGRAM

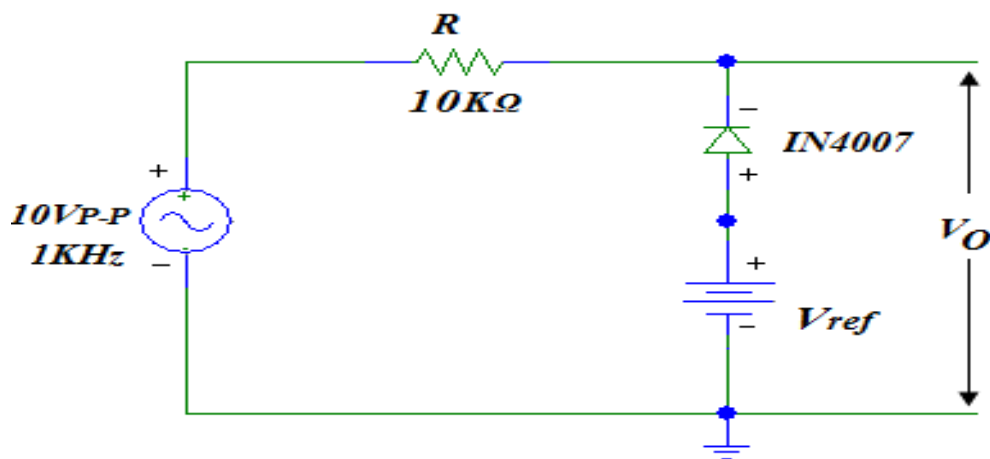


Fig 6(A).2.a Shunt clipper for clipping below the reference level.

DESIGN

Let the output voltage be clipped at say $V_o = +4V$

Therefore $V_o(\min) = +4V$

From Fig 6(B).2.a above, $V_o(\min) = -V_f + V_{ref}$ (Where $V_f = V_K = V_f$ cut in voltage of the diode $\approx 0.6V$)

Therefore $V_{ref} = V_o(\min) + V_f = 4 + 0.6 = 4.6V$

The value of resistor R is designed usually by equation $R = \sqrt{R_f R_r}$

Where R_f = diode forward resistance = 10Ω

and R_r = diode reverse resistance = $10M\Omega$

Therefore $R = \sqrt{10 \times 10 \times 10^6} = 10K\Omega$

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(A).2.a
2. Switch on the VRPS and set the supply voltage $V_{ref} = 4.6V$
3. Apply a Sine Wave input (V_{in}) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply V_{in} and V_o to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

OUTPUT WAVEFORM

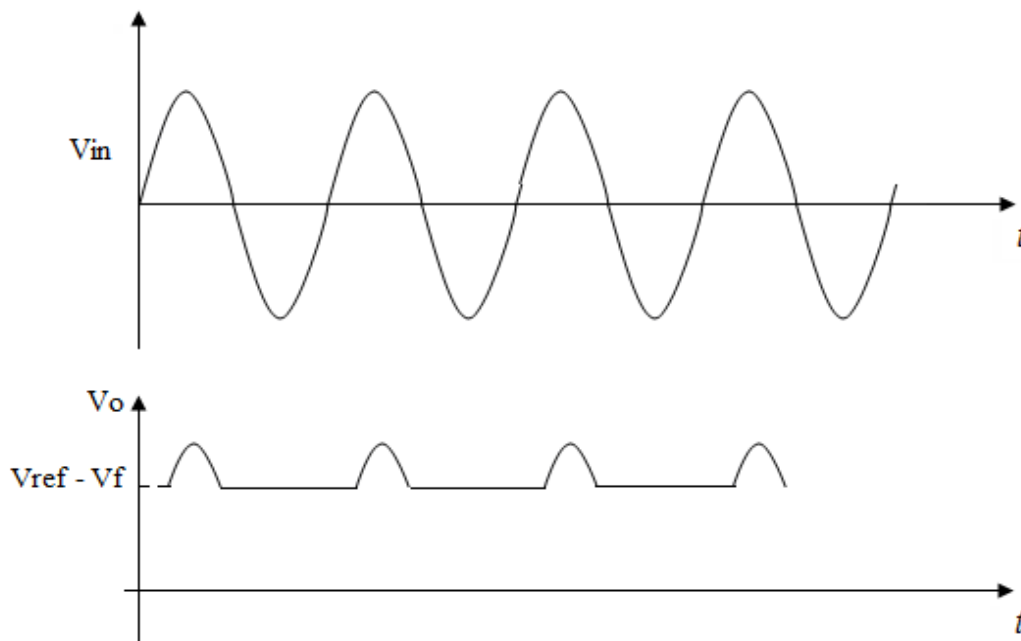


Fig 6(A).2.b Wave form of shunt clipper for clipping below reference level.

TRANSFER CHARACTERISTICS

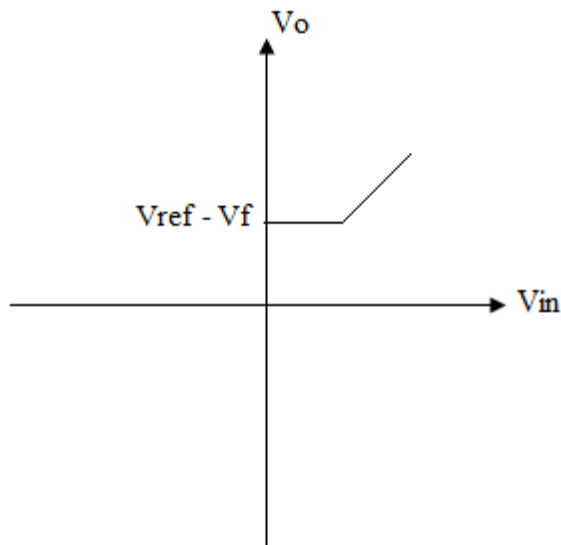


Fig 6(A).2.c Transfer characteristics of shunt clipper for clipping below reference level.

6(B) DOUBLE ENDED SHUNT CLIPPING CIRCUITS

6(B).1 CLIPPING AT TWO POSITIVE ENDS (ASYMMETRICAL CLIPPER)

CIRCUIT DIAGRAM

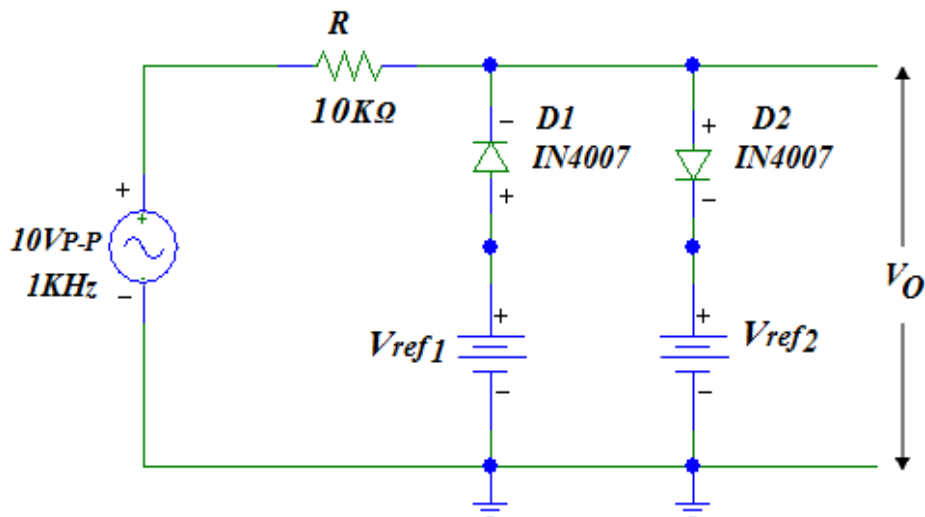


Fig 6(B).1.a Two level clipping circuit.

DESIGN

Let the output voltage be clipped at say $V_o(\text{max}) = +6\text{V}$ and $V_o(\text{min}) = +3\text{V}$

Let $V_{\text{ref2}} > V_{\text{ref1}}$

We have $V_o(\text{max}) = 6\text{V}$

We have from Fig 7(B).1.a above, $V_o(\text{max}) = V_{\text{ref2}} + V_f$ Where V_f is diode D2 cut in voltage $\approx 0.6\text{V}$

Therefore **$V_{\text{ref2}} = V_o(\text{max}) - V_f = 6 - 0.6 = 5.4\text{V}$**

Also we have $V_o(\text{min}) = 3\text{V}$

We have from Fig 7(B).1.a above, $V_o(\text{min}) = V_{\text{ref1}} - V_f$ Where V_f is diode D2 cut in voltage $\approx 0.6\text{V}$

Therefore **$V_{\text{ref1}} = V_o(\text{min}) + V_f = 3 + 0.6 = 3.6\text{V}$**

The value of resistor R is designed usually by equation $R = \sqrt{R_f R_r}$

Where $R_f =$ diode forward resistance $= 10\Omega$

and $R_r =$ diode reverse resistance $= 10\text{M}\Omega$

Therefore **$R = \sqrt{10 \times 10 \times 10^6} = 10\text{K}\Omega$**

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(B).1.a
2. Switch on the VRPS and set the supply voltage $V_{\text{ref1}} = 6.6\text{V}$ and $V_{\text{ref2}} = 5.4\text{V}$
3. Apply a Sine Wave input (V_{in}) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform, Output waveform and clipping level in CRO.
5. Apply V_{in} and V_o to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO.

OUTPUT WAVEFORMS

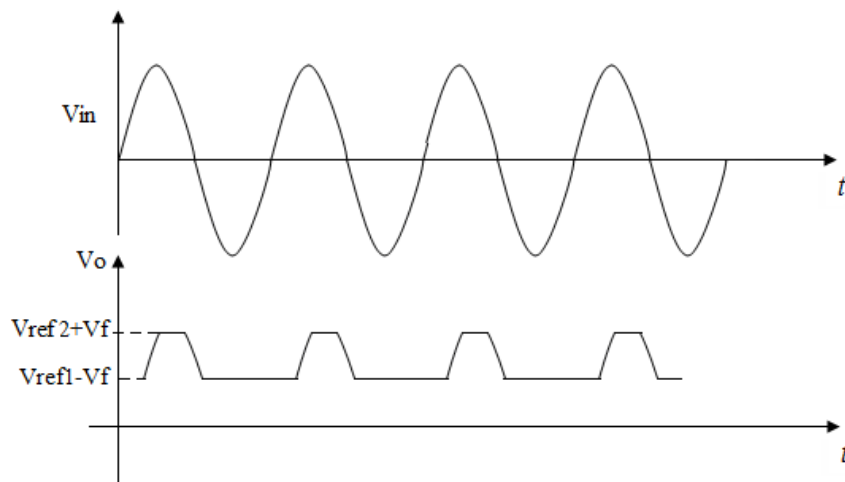


Fig 6(B).1.b Wave form of a Two level clipper.

TRANSFER CHARACTERISTICS

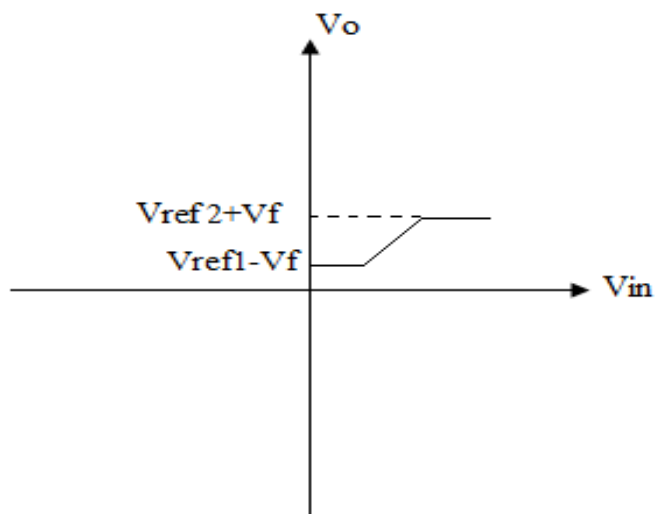


Fig 6(B).1.c Transfer characteristics of two level clipper.

6(B).2 CLIPPING AT TWO INDEPENDENT LEVELS (SYMMETRICAL CLIPPER)

CIRCUIT DIAGRAM

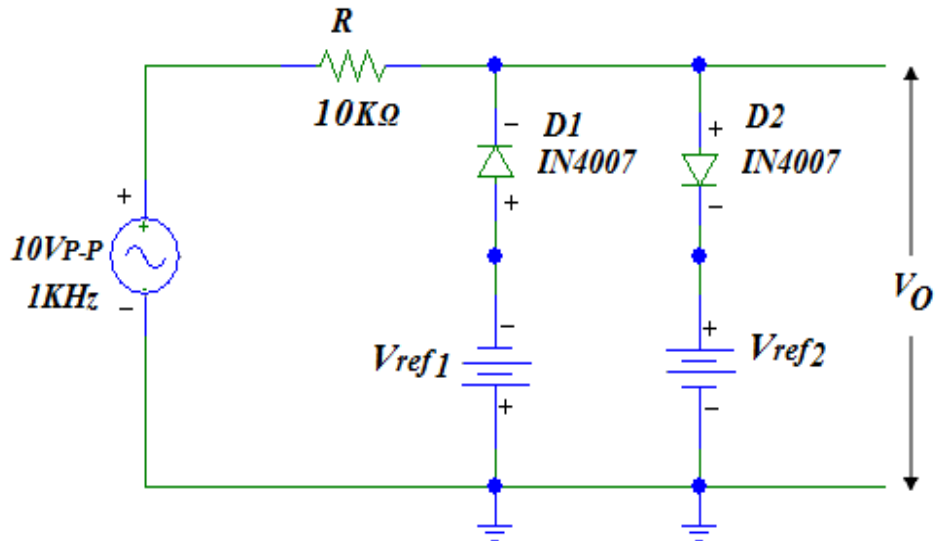


Fig 6(B).2.a Two level clipper to clip at two independent level.

DESIGN

Let the output voltage be clipped at say $V_o(\max) = +6V$ and $V_o(\min) = -6V$

We have, $V_o(\max) = 6V$

We have from Fig 7(B).2.a above, $V_o(\max) = V_{ref2} + V_f$ Where V_f is diode $D2$ cut in voltage $\approx 0.6V$

Therefore $V_{ref2} = V_o(\max) - V_f = 6 - 0.6 = 5.4V$

Also we have $V_o(\min) = -6V$

We have from Fig 7(B).1.a above, $V_o(\min) = -V_{ref1} - V_f$ Where V_f is diode $D1$ cut in voltage $\approx 0.6V$

Therefore $V_{ref1} = -V_o(\min) + V_f = -(-6) + 0.6 = 6.6V$

The value of resistor R is designed usually by equation $R = \sqrt{R_f R_r}$

Where R_f = diode forward resistance = 10Ω

and R_r = diode reverse resistance = $10M\Omega$

Therefore $R = \sqrt{10 \times 10 \times 10^6} = 10K\Omega$

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(B).2.a
2. Switch on the VRPS and set the supply voltage $V_{ref1} = -5.4V$ and $V_{ref2} = 5.4V$
3. Apply a Sine Wave input (V_{in}) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply V_{in} and V_o to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

OUTPUT WAVEFORM

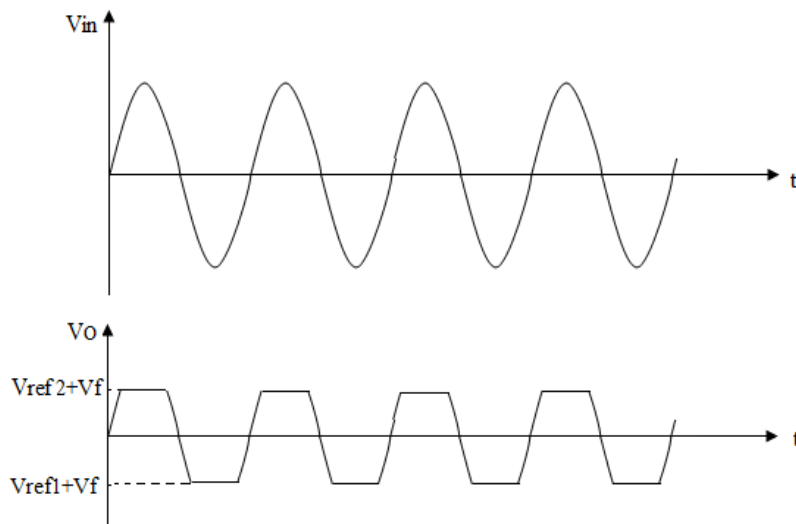


Fig 6(B).2.b wave form of two level clipper to clip at two independent level

TRANSFER CHARACTERISTICS

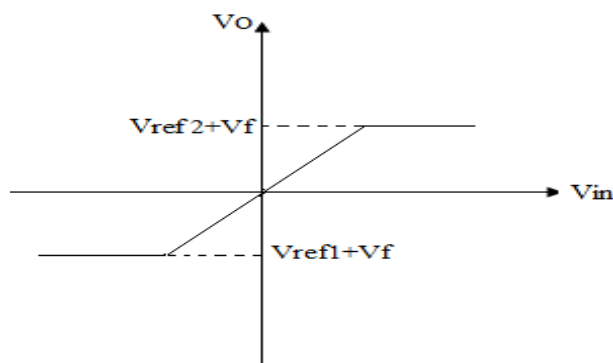


Fig 6(B).2.c Transfer characteristics of two level clipper to clip at two independent level.

RESULT: Diode Clipper Circuits designed and verified

EXPECTED VIVA QUESTIONS

1. What is Semiconductor?
2. What is Intrinsic Semiconductor?
3. What is extrinsic Semiconductor?
4. What is p-n junction?
5. What is doping?
6. What is knee voltage?
7. What is breakdown voltage?
8. What is peak inverse voltage (PIV) of diode?
9. What is the maximum power rating?
10. What is the drift current?
11. What is diffusion current?.
12. What is diffusion capacitance?
13. In what condition of the diode diffusion capacitance occurs?
14. What is diode?
15. What are the characteristics of ideal diode, when it is forward bias?
16. What are the characteristics of ideal diode when it is reverse biased?

OBSERVATION AND WORK SHEET

3 GRAPH SHEETs HAVE TO BE INSERTED

EXPERIMENT NO.7**DIODE CLAMPING CIRCUITS.****AIM**

To Design and Verify positive and negative clamping circuits.

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Capacitor	0.1 μ F	1
04	VRPS	0-30Vdc 3A	1
05	CRO for testing		1
06	Probes, wires		1
07	Digital multimeter		1

THEORY

Clamper is a circuit that "clamps" a signal to a different DC level without changing the appearance (or Shape) of the applied signal. The different types of clampers are positive , negative and biased clampers. A clamping network must have a capacitor, a diode and a resistive element. The magnitude of R and C must be chosen such that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is not conducting. By connecting suitable DC voltage in series with the diode, the level of swing can be varied.

A circuit that places either the Positive or Negative peak of a signal at a desired fixed DC level is known as clamping circuit. A clamping circuit essentially adds DC to the input A.C signal. In positive clamper the input signal is a square wave having a peak value of V (volts). The clamper adds the DC component and pushes the signal upwards so that the negative peaks fall on the zero level. It may be seen that the shape of the original signal has not changed, only there is vertical shift in the signal .Such a clamper is called a positive clamper. The negative clamper does the reverse that is it pushes the signal downwards so that positive peak fall on the zero level. A clamping circuit should not change peak to peak value of the signal. It should only change the DC level. To do so, a clamping

circuit uses a capacitor, together with a diode and a load resistor R_L . The operation of a clamper is based on the principle that charging time of a capacitor is made very small as compared to its discharging time.

**7(A) POSITIVE CLAMPING CIRCUIT WITH REFERENCE VOLTAGE(V_{ref})
OR NEGATIVE PEAK CLAMPER WITH REFERENCE VOLTAGE(V_{ref})**

CIRCUIT DIAGRAM

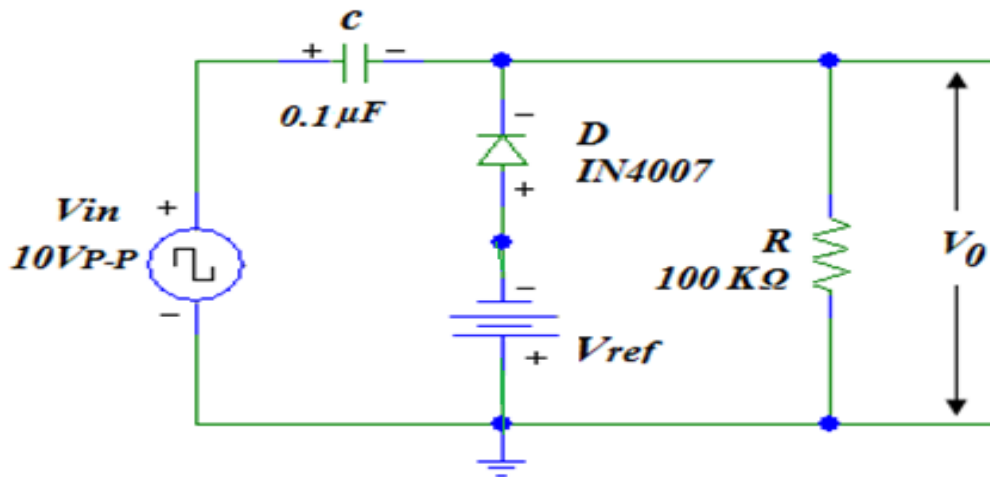


Fig 7(A).a Positive clamper with V_{ref}

DESIGN

Let negative peak be clamped at $V_o(\min) = -4V$

From Fig given above, $V_o(\min) = -V_{ref} - V_\gamma$

Therefore $V_{ref} = -V_o(\min) - V_\gamma = -(-4) - 0.6 = 3.4V$

Let input frequency = 1KHz. Therefore $T = 1 / f = 1 \text{ ms}$.

Let $RC = 10T$ (because discharge time of the capacitor should be $\gg T$)

Let $R = 100K\Omega$, therefore $C = 10 \text{ ms} / 100K\Omega = 0.1\mu F$.

So use $R = 100K\Omega$ and $C = 0.1\mu F$.

PROCEDURE

1. Rig up the circuit as shown in the circuit diagram.
2. Set the input to 10V(p-p) square wave.
3. Select the input signal V_{in} amplitude to 10V(p-p) and 1kHz frequency.

4. Observe and verify the output waveform.

INPUT AND OUTPUT WAVEFORMS

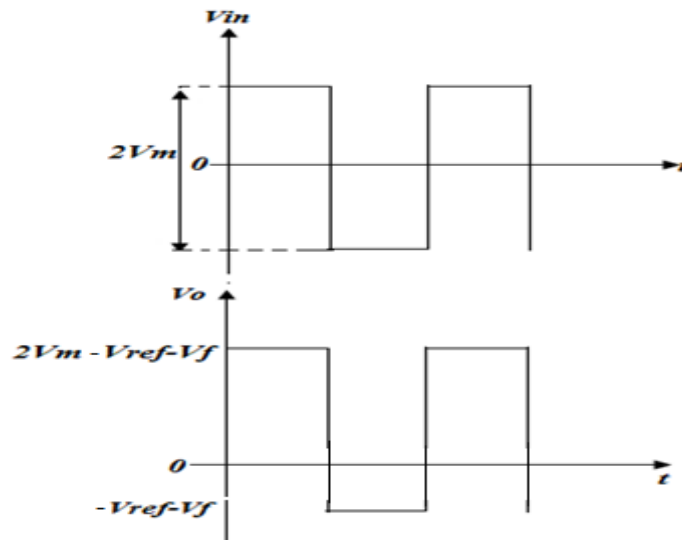


Fig.7(A).b Waveforms of positive clamper with V_{ref}

7(B) NEGATIVE CLAMPING CIRCUIT WITH REFERENCE VOLTAGE(V_{ref}) OR POSITIVE PEAK CLAMPER WITH REFERENCE VOLTAGE(V_{ref})

CIRCUIT DIAGRAM

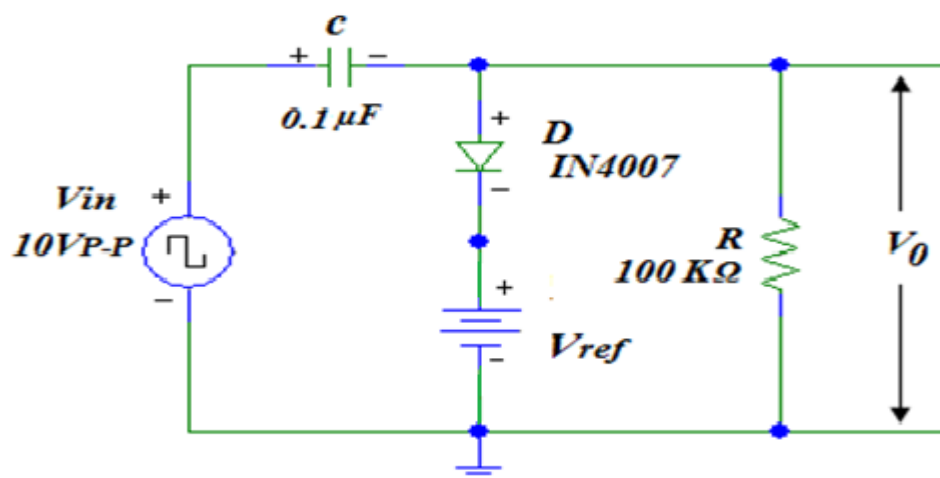


Fig 7(B).a Negative clamper with V_{ref}

DESIGN

Let positive peak be clamped at $V_o(\max)=+4V$

From Fig given above , $V_o(\max)=V_{ref} + V_\gamma$

Therefore $V_{ref}=V_o(\max) - V_\gamma = 4 - 0.6 = 3.4V$

Let input frequency = 1KHz .Therefore $T = 1 / f = 1 \text{ ms}$.

Let $RC=10T$ (because discharge time of the capacitor should be $\gg T$)

Let $R=100K\Omega$, therefore $C=10 \text{ ms} / 100K\Omega = 0.1\mu F$.

So use $R=100K\Omega$ and $C=0.1\mu F$.

PROCEDURE

1. Rig up the circuit as shown in the circuit diagram.
2. Set the input to 10V(p-p) square wave.
3. Select the input signal V_{in} amplitude to 10V(p-p) and 1kHz frequency.
4. Observe and verify the output waveform.

INPUT AND OUTPUT WAVEFORMS

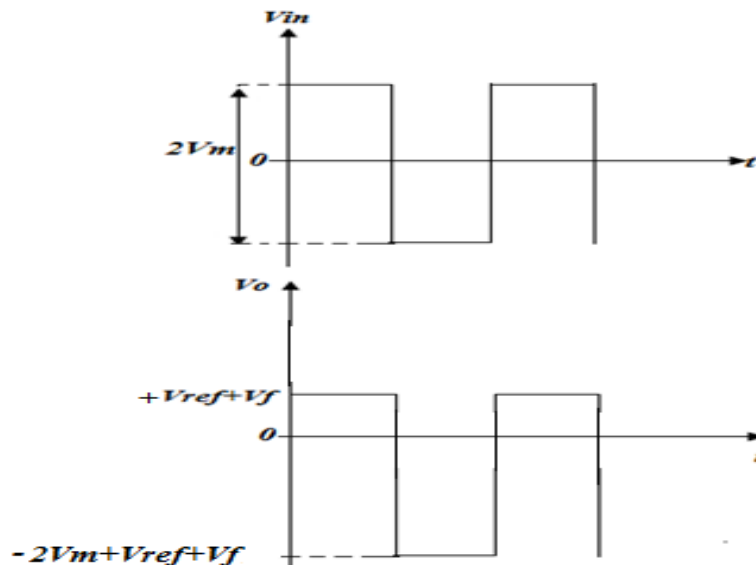


Fig.7(B).b Waveforms of negative clamper with V_{ref}

RESULT

Both the positive and negative clamping circuits are designed and observed the variation in the swing as DC voltage varies.

EXPECTED VIVA QUESTIONS

1. What is Semiconductor?
2. What is an Intrinsic Semiconductor?
3. What is an extrinsic Semiconductor?
4. What is a p-n junction?
5. What is doping?
6. What is the knee voltage of a diode?
7. What is breakdown voltage?
8. What is peak inverse voltage (PIV) of a diode?
9. What is the maximum power rating a diode?
10. What is drift current?
11. What is diffusion current?
12. What is diffusion capacitance?
13. In what condition of the diode diffusion capacitance occurs?
14. What is a diode? What the name diode stands for?
15. What are the characteristics of an ideal diode when it is forward biased?
16. What are the characteristics of an ideal diode when it is reverse biased?
17. Define clamping.
18. Mention different types of clamping circuits.
19. What are the applications of clamping circuits?

OBSERVATION AND WORK SHEET

2 GRAPH SHEETS HAS TO BE INSERTED

EXPERIMENT NO. 8**CLASS B PUSH PULL POWER AMPLIFIER****AIM**

To determine the conversion efficiency of Transformer Less class B complementary symmetry push pull power amplifier.

COMPONENTS REQUIRED

Sl. No	Apparatus and components	Range	Quantity
01	Bread board		1
02	Transistor	SL100,SK100	1+1
03	Resistors	470 Ω	2
04	Capacitors	0.47 μ F ,47 μ F	2+1
05	VRPS	0-30V DC, 3A	
06	Signal generator	10Hz to 3M Hz	1
07	CRO for testing		1
08	Probes, wires		2+10
09	DRB	0 to1M Ω	1
10	Multimeter for testing		2

THEORY

The power amplifier is a device that converts dc power into ac power and the output is controlled by the input signal.

In class B power amplifier, the Q point is located at cutoff. This means that the base emitter voltage is at zero volts. As a result the transistor conducts for one half cycle of the single cycle. To obtain output for full cycle of the signal it is necessary to use two transistors,one conducts during the positive half cycle and the other conducts during the negative half cycle .Conversion efficiency is a measure of the ability of an active device to convert the dc power of supply into the ac power delivered to the load is called the conversion efficiency. Theoretically the efficiency of the class B push pull amplifier operation is about 78.5%.

CIRCUIT DIAGRAM

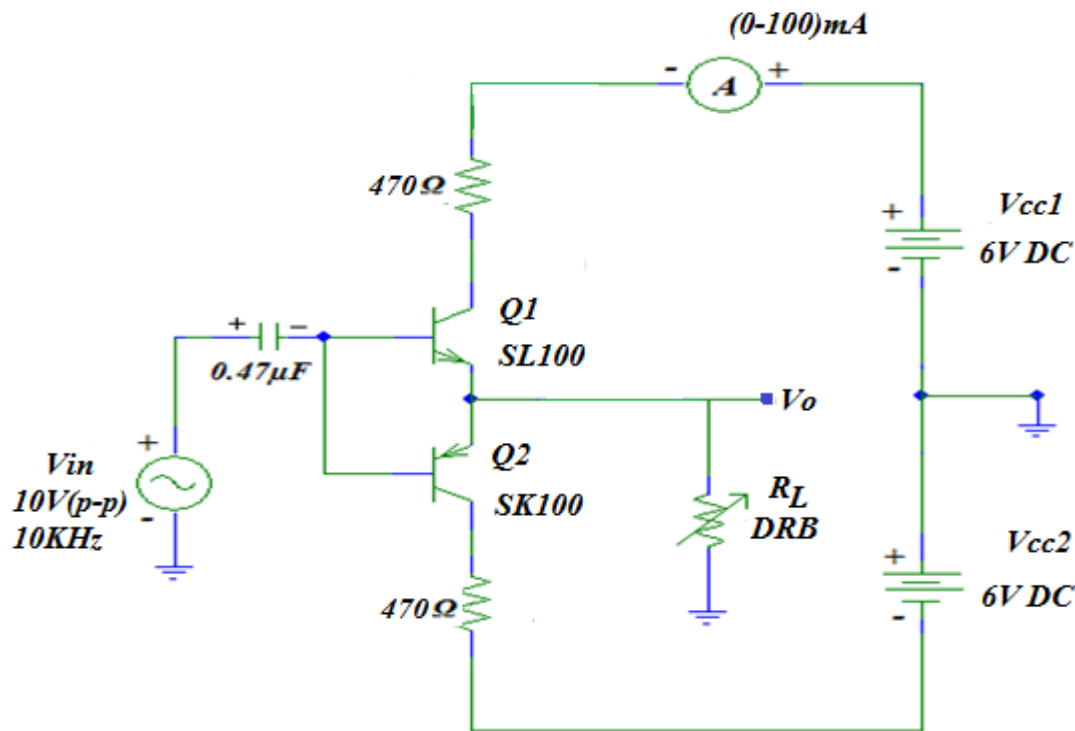


Fig 8.a – Class B power amplifier

PROCEDURE

1. Rig up the circuit as shown in figure 8.a.
2. Switch on the power supplies and adjust the supply voltages $V_{cc1}=V_{cc2}=V_{cc}=6\text{ V}$.
3. Apply the sinusoidal signal of frequency say 10 KHz, from the signal generator and vary the amplitude till maximum undistorted output is obtained and observe the cross-over distortion.
4. Note down the peak to peak amplitude of the output waveform ($V_o(p-p)$) and DC collector current I_c shown by the ammeter for a particular value of load resistor R_L and record the readings as shown in the tabular column.
5. Repeat the procedure for different values of load resistor R_L , note down the output voltage $V_o(p-p)$, I_{DC} and determine the conversion efficiency.

$$V_{cc1} = V_{cc2} = 6V$$

$$V_{in} = 10V_{p-p} \text{ (at 10KHz)}$$

RESULT

The maximum practical conversion efficiency of Transformer Less class B complementary symmetry push pull power amplifier = _____ at optimum load R_L = _____

EXPECTED VIVA QUESTIONS

1. What is a Class B push pull amplifier?
2. Why it is called as push pull amplifier?
3. What type of transistor is used in push pull amplifier?
4. Mention the different types of distortions in power amplifiers.
5. Define harmonic distortion.
6. What is the conversion efficiency of Class B push pull amplifier ?
7. How are power amplifiers classified?
8. Mention different types of power amplifiers.
9. What are the applications of power amplifiers?

OBSERVATION AND WORK SHEET

EXPERIMENT NO.9**RECTIFIER CIRCUITS****9(A) HALF WAVE RECTIFIER CIRCUITS****AIM**

To study half wave rectifier circuits with and without filter and to calculate ripple factor and efficiency.

COMPONENTS REQUIRED:

Sl. No	Apparatus	Range	Quantity
01	Bread board		1
02	Diode	1N4007	1
03	Capacitor	47 μ F	1
04	VRPS	0-30V DC, 3A	1
05	CRO for testing		1
06	Probes, wires		1
07	Digital multimeter		2
08	DRB		1

THEORY

A rectifier converts AC to pulsating DC. Rectifiers are used in the design of dc power supplies required for all electrical circuits to work. A semiconductor diode conducts only in one direction. This property is used in the design of rectifier circuit. Based on the output there are mainly two types of rectifiers namely half wave and full wave rectifiers. As the DC output voltage is in pulsed form to get pure DC, capacitor is used to filter it.

Half wave rectifiers: The Half wave rectifier is a circuit, which converts an ac voltage to dc voltage. Rectification takes place for only half cycle of the input.

In the Half wave rectifier circuit the transformer serves two purposes.

1. It can be used to obtain the desired level of AC voltage (using step up or step down transformers).
2. It provides isolation from the power line.

The primary of the transformer is connected to ac supply. This induces an ac voltage across the secondary of the transformer. During the positive half cycle of the input voltage the polarity of the voltage across the secondary forward biases the diode. As a result a current will flows through the load resistor R_L . The forward biased diode offers a very low resistance and hence the voltage drop across it is very small. Thus the voltage appearing across the load is practically the same as the input voltage at every instant. During the negative half cycle of the input voltage the polarity of the voltage across the secondary reversed biases the diode. As a result a current will not flows through the load resistor R_L . The reversed biased diode offers a very high resistance and hence the voltage drop across it is very high. Thus the voltage appearing across the load is practically the zero voltage at every instant negative half cycle of the input voltage. Thus it rectifies only half of the input signal. so it is called as half wave rectifier.

Full wave rectifier: Both cycles are rectified and ripple factor will be less and efficiency increases. Based on the construction, there are mainly two types of full wave rectifiers:-

- Center tap full wave rectifier:** In this configuration, only 2 diodes are sufficient, but transformer with center tap secondary is must. Peak inverse voltage of the diode is twice the input voltage.
- Full wave bridge rectifier:** Four diodes are required and can be applied without transformer also. As two diodes are in series for each half cycle, the voltage drop across the diode is twice that of the center tap transformer. So at very low voltage this is not suitable.

9(A).1 HALF WAVE RECTIFIER WITHOUT CAPACITOR FILTER

CIRCUIT DIAGRAM

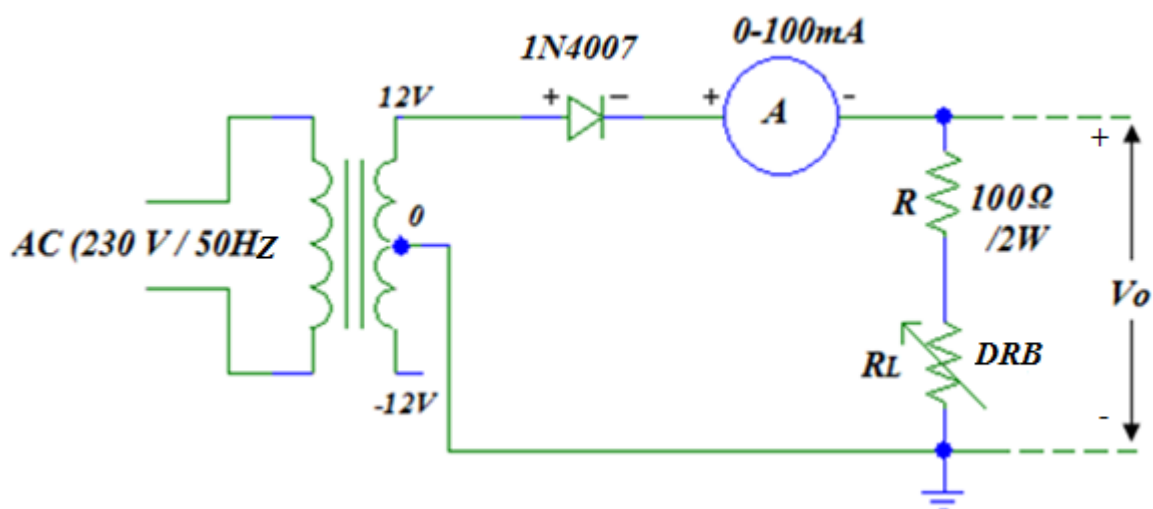


Fig 9(A).1.a Half wave rectifier circuit.

DESIGN

Let output DC voltage and current required i.e, $V_{dc}=5V$ and $I_{dc}=I_{L(max)}=50mA$ respectively.

Output voltage DC voltage is given by $V_{dc} = I_{dc} R_L$

So $R_L = V_{dc} / I_{dc} = 5 / 50mA = 100\Omega$

Power dissipated in R_L is , $P_L = V_{dc} I_{L(max)} = 5 \times 50 \times 10^{-3} = 0.25$ Watts

For R_L use $100\Omega/0.5W$ in series with DRB

For Half wave rectifier , $V_{dc} = V_m / \pi$

$V_m = V_{dc} \pi = 5\pi = 15.7V$ Where V_m = peak value of transformer secondary voltage

$V_{rms} = V_m / \sqrt{2} = 15.7 / \sqrt{2}$ Where V_{rms} = peak value of transformer secondary voltage

$\Rightarrow V_{rms}=11.10V$

Select 12V secondary (12V-0-12V transformer)

FORMULAE

DC Output Power , $P_{dc} = (I_{dc}^2 * R_L)$

AC Input Power , $P_{ac} = [(I_{rms})^2 * (R_L + R_F)]$, Where R_F is diode forward resistance

Assume $R_F=10\Omega$

Efficiency η = Output DC power / Input AC power

$\% \eta = (P_{dc} / P_{ac}) * 100$

$\% \text{ Regulation} = [(V_{dc(NL)} - V_{dc(FL)} / V_{dc(FL)}] * 100$

Ripple factor $\gamma = V_{ac} / V_{dc}$ or I_{ac} / I_{dc}

PROCEDURE

1. Test the transformer and observe the secondary waveform in CRO.
2. Connect circuit the secondary as shown in the Fig 9(A).1.a.
3. Observe the waveform on CRO across the load resistor which appears as in fig given below.
4. Set the DRB(Load Resistance) to maximum and note down value of currents I_{dc} and I_{ac} with

the same multimeter (using proper ranges and modes(i.e, AC or DC)). Also note down the value of voltages V_{dc} and V_{ac} with the same multimeter (using proper ranges and modes). The value of V_{dc} for DRB set to maximum is designated as $V_{dc(NL)}$ (No Load Voltage).

5. Vary I_{dc} in steps by varying DRB and measure corresponding values of I_{dc} , V_{dc} , V_{ac} and record the readings as shown in Table 9(A).1.a .
6. Measure V_m from CRO ($V_{dc}=V_m / \pi$).
7. Measure V_{ac} across the load.
8. Find ripple = V_{ac} / V_{dc} .
9. Measure I_{dc} and I_{rms} .
10. Find efficiency $\% \eta$.
11. Open circuit the load and measure no load voltage $V_{dc(NL)}$ (i.e, set DRB to maximum).
12. Measure full load Voltage $V_{dc(FL)}$ (i.e, set DRB to some low resistance 100Ω , 200Ω etc).
13. Find the percentage regulation $\%R$.
14. Calculate the Ripple Factor and Efficiency for each load resistance.

OUTPUT WAVEFORM

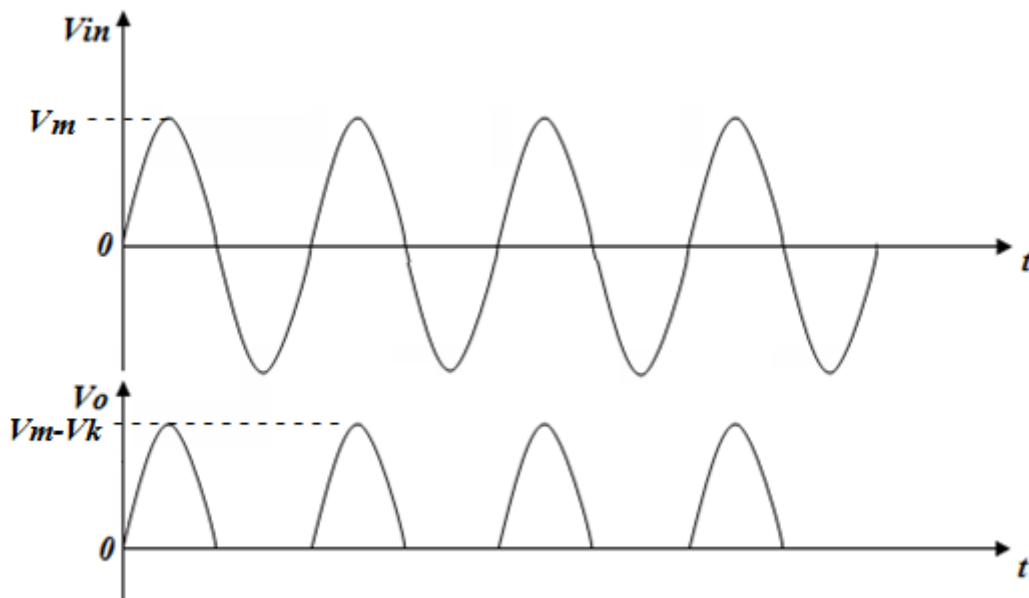


Fig 9(A).1.b Wave forms of Half wave rectifier.

TABULAR COLUMN

$R_L(\text{ohms})$	$I_{dc}(\text{mA})$	$V_{dc}(\text{V})$	$V_{ac}(\text{V})$	$I_{ac}(\text{mA})$	Efficiency $\% \eta$	Ripple $\gamma = V_{ac}/V_{dc}$	Regulation $\% R$

Table 9(A).1.a To record the experimental values of Half wave rectifier.

9(A).2 HALF WAVE RECTIFIER WITH CAPACITOR FILTER

CIRCUIT DIAGRAM

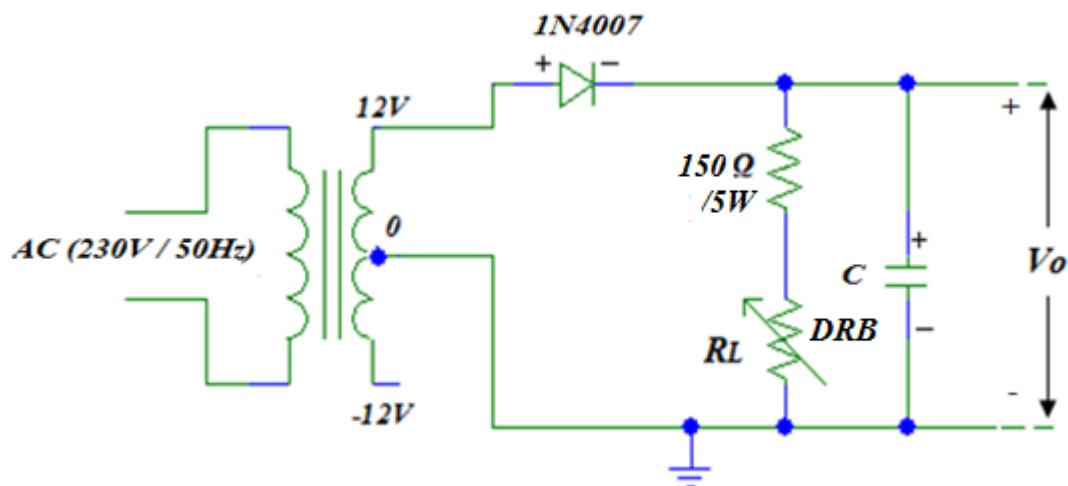


Fig 9(A).2.a Half wave rectifier circuit with capacitor filter.

DESIGN

Let output DC voltage and current required i.e, $V_{dc}=5V$ and $I_{dc}=I_{L(max)}=50mA$ respectively.

Let Ripple factor $\gamma \leq 0.08$

Output voltage DC voltage is given by $V_{dc} = I_{dc} R_L$

So $R_L = V_{dc} / I_{dc} = 5V / 50mA = 100\Omega$

Power dissipated in R_L is , $P_L = V_{dc} I_{L(max)} = 5 \times 50 \times 10^{-3} = 0.25$ Watts

For R_L use $150\Omega/0.5W$ in series with DRB

For Half wave rectifier , $V_{dc} = V_m / \pi$

$V_m = V_{dc} \pi = 5\pi = 15.7V$ Where V_m = peak value of transformer secondary voltage

$V_{rms} = V_m / \sqrt{2} = 15.7 / \sqrt{2}$ Where V_{rms} = peak value of transformer secondary voltage

$\Rightarrow V_{rms} = 11.10V$

Select 12V secondary (12V-0-12V transformer)

DESIGN FOR THE CAPACITOR FILTER

Given ripple factor $\gamma = 0.08$

Ripple factor $\gamma = 1 / 2\sqrt{3}f R_L C$ We have $f = 50Hz$

Therefore $C = 1 / (2 \times \sqrt{3} \times 50 \times 100 \times 0.08) = 721.6\mu F$

Use $C = 700\mu F$ a standard value

Ripple = $1 / 2\sqrt{3}fRC$ where, $R = R_L + R$. Choose $R_L = 100\Omega$, $c = 47\mu F$ and $f = 50Hz$

FORMULAE

DC Output Power , $P_{dc} = (I_{dc}^2 * R_L)$

AC Input Power , $P_{ac} = [(I_{rms})^2 * (R_L + R_F)]$, Where R_F is diode forward resistance

Assume $R_F = 10\Omega$

Efficiency $\eta = \text{Output DC power} / \text{Input AC power}$

$\% \eta = (P_{dc} / P_{ac}) * 100$

$$\% \text{ Regulation} = [(V_{dc(NL)} - V_{dc(FL)} / V_{dc(FL)}] * 100$$

$$\text{Ripple factor } \gamma = V_{ac} / V_{dc} \text{ or } I_{ac} / I_{dc}$$

PROCEDURE

1. Test the transformer and observe the secondary waveform in CRO.
2. Connect circuit the secondary as shown in the Fig 9(A).2.a
3. Observe the waveform on CRO across the load resistor which appears as in fig given below.
4. Set the DRB(Load Resistance) to maximum and note down value of currents I_{dc} and I_{ac} with the same multimeter (using proper ranges and modes(i.e, AC or DC). Also note down the value of voltages V_{dc} and V_{ac} with the same multimeter (using proper ranges and modes). The value of V_{dc} for DRB set to maximum is designated as $V_{dc(NL)}$ (No Load Voltage).
5. Vary I_{dc} in steps by varying DRB and measure corresponding values of I_{dc} , V_{dc} , V_{ac} and record the readings as shown in Table 9(A).2.a .
6. Measure V_m from CRO ($V_{dc} = V_m / \pi$).
7. Measure V_{ac} across the load.
8. Find ripple = V_{ac} / V_{dc} .
9. Measure I_{dc} and I_{rms} .
10. Find efficiency $\% \eta$.
11. Open circuit the load and measure no load voltage $V_{dc(NL)}$ (i.e, set DRB to maximum).
12. Measure full load Voltage $V_{dc(FL)}$ (i.e, set DRB to some low resistance 100Ω , 200Ω etc).
13. Find the percentage regulation $\%R$.
14. Calculate the Ripple Factor and Efficiency for each load resistance.

OUTPUT WAVEFORMS

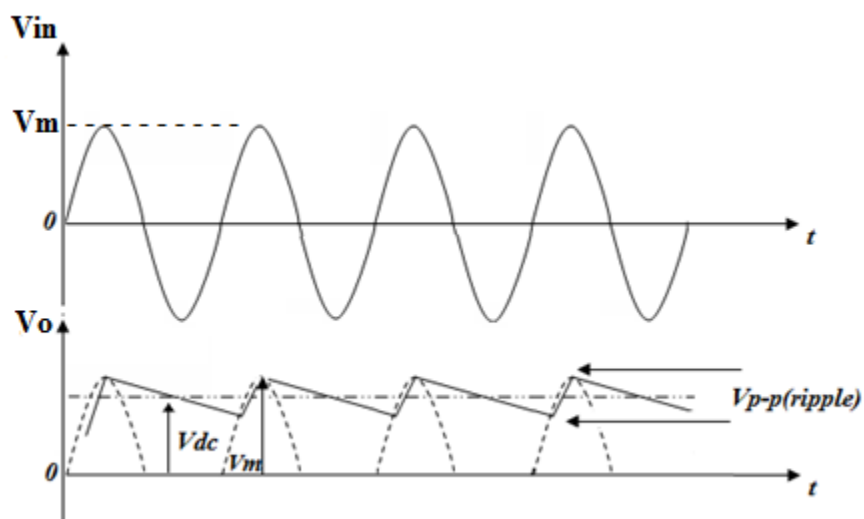


Fig 9(A).2.b Wave forms of Half wave rectifier with capacitor filter.

TABULAR COLUMN

$R_L(\text{ohms})$	$I_{dc}(\text{mA})$	$V_{dc}(\text{V})$	$V_{ac}(\text{V})$	$I_{ac}(\text{mA})$	Efficiency $\% \eta$	Ripple $\gamma = V_{ac}/V_{dc}$	Regulation $\% R$

Table 9(A).2.a to record the experimental values of Half wave rectifier with capacitor filter.

$$V_{DC} = V_m - (V_{p-p} \text{ Ripple} / 2)$$

$$V_{rms} = V_{p-p} \text{ Ripple} / 2\sqrt{3}$$

RESULT

	Ripple factor value	Efficiency	Regulation
HWR without filter			
HWR with filter			

OBSERVATION AND WORK SHEET

9(B) FULL WAVE RECTIFIER CIRCUITS**AIM**

To study full wave rectifier circuit with and without filter and to calculate ripple factor and efficiency.

COMPONENTS REQUIRED

Sl. No	Apparatus	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Capacitor	47 μ F	1
04	VRPS	0-30Vdc 3A	1
05	CRO for testing		1
06	Probes, wires		1
07	Digital multimeter		2
08	DRB		1

THEORY

A rectifier converts ac to pulsating dc. Rectifiers are used in the design of dc power supplies required for all electrical circuits to work. A semiconductor diode conducts only in one direction. This property is used in the design of rectifier circuit. Based on the output there are mainly two types of rectifiers namely half wave and full wave rectifiers. As the Dc output voltage is in pulsed form, capacitor is used to filter it.

Full wave rectifier: Both cycles are rectified and ripple factor will be less and efficiency increases. Based on the construction, there are mainly two types of full wave rectifiers:-

- a) **Center tap full wave rectifier:** In this configuration, only 2 diodes are sufficient, but transformer with center tap secondary is must. Peak inverse voltage of the diode is twice the input voltage.
- b) **Full wave bridge rectifier:** Four diodes are required and can be applied without transformer also. As two diodes are in series with each cycle, the voltage drop across the diode is twice that of in the center tap transformer. So at very low voltage this is not suitable.

9(B).1 FULL WAVE RECTIFIER WITHOUT CAPACITOR FILTER

CIRCUIT DIAGRAM

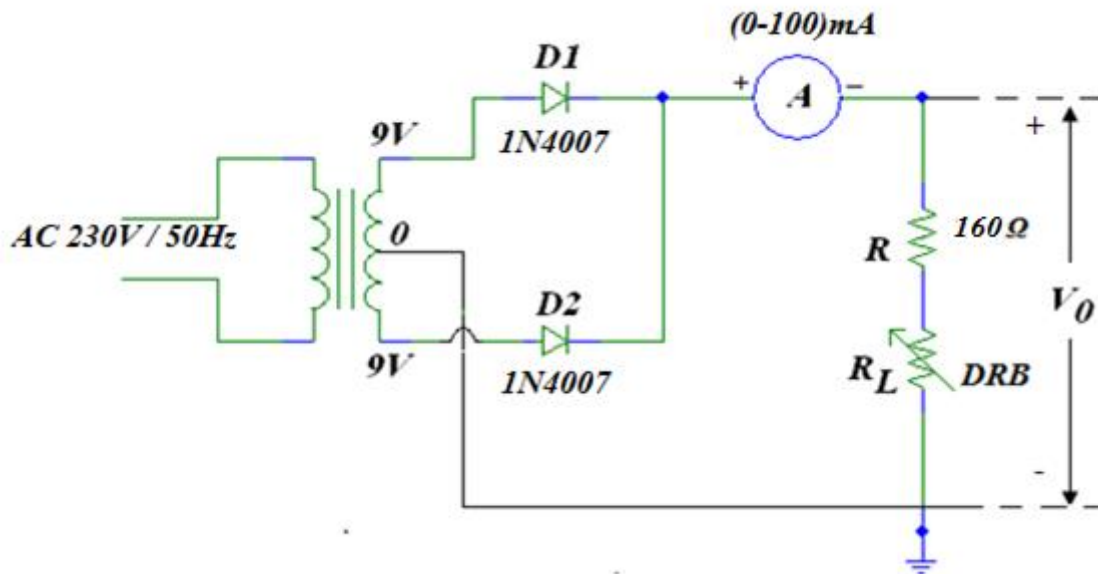


Fig 9(B).1.a Full wave rectifier circuit.

DESIGN

Let output DC voltage and current required i.e, $V_{dc}=8V$ and $I_{dc}=I_{L(max)}=50mA$ respectively.

Output voltage DC voltage is given by $V_{dc} = I_{dc} R_L$

So $R_L = V_{dc} / I_{dc} = 8V / 50mA = 160\Omega$

Power dissipated in R_L is , $P_L = V_{dc} I_{L(max)} = 8 \times 50 \times 10^{-3} = 0.4 \text{ Watts}$

For R_L use $160\Omega/0.5W$ in series with DRB

For Half wave rectifier , $V_{dc} = 2V_m / \pi$

$V_m = V_{dc} \pi / 2 = 8\pi / 2 = 12.56V$ Where V_m = peak value of transformer secondary voltage

$V_{rms} = V_m / \sqrt{2} = 12.56 / \sqrt{2}$ Where V_{rms} = peak value of transformer secondary voltage

$\Rightarrow V_{rms}=9V$

Select 9V secondary (9V-0-9V transformer)

FORMULAE

DC Output Power , $P_{dc} = (I_{dc})^2 R_L$

AC Input Power , $P_{ac} = (I_{rms})^2 (R_L + R_F)$, Where R_F is diode forward resistance

Assume $R_F = 10\Omega$

Efficiency η = Output DC power / Input AC power

$\% \eta = (P_{dc} / P_{ac}) * 100$

$\% \text{ Regulation} = [(V_{dc(NL)} - V_{dc(FL)} / V_{dc(FL)}] * 100$

Ripple factor $\gamma = V_{ac} / V_{dc}$ or I_{ac} / I_{dc}

PROCEDURE

1. Test the transformer and observe the secondary waveform in CRO.
2. Connect circuit the secondary as shown in the Fig 9(B).1.a.
3. Observe the waveform on CRO across the load resistor which appears as in fig given below.
4. Set the DRB(Load Resistance) to maximum and note down value of currents I_{dc} and I_{ac} with the same multimeter (using proper ranges and modes(i.e, AC or DC). Also note down the value of voltages V_{dc} and V_{ac} with the same multimeter (using proper ranges and modes). The value of V_{dc} for DRB set to maximum is designated as $V_{dc(NL)}$ (No Load Voltage).
5. Vary I_{dc} in steps by varying DRB and measure corresponding values of I_{dc} , V_{dc} , V_{ac} and record the readings as shown in Table 9(B).1.a .
6. Measure V_m from CRO ($V_{dc} = V_m / \pi$).
7. Measure V_{ac} across the load.
8. Find ripple = V_{ac} / V_{dc} .
9. Measure I_{dc} and I_{rms} .
10. Find efficiency $\% \eta$.
11. Open circuit the load and measure no load voltage $V_{dc(NL)}$ (i.e, set DRB to maximum).
12. Measure full load Voltage $V_{dc(FL)}$ (i.e, set DRB to some low resistance 100Ω , 200Ω etc).

13. Find the percentage regulation %R.

14. Calculate the Ripple Factor and Efficiency for each load resistance.

OUTPUT WAVEFORMS:

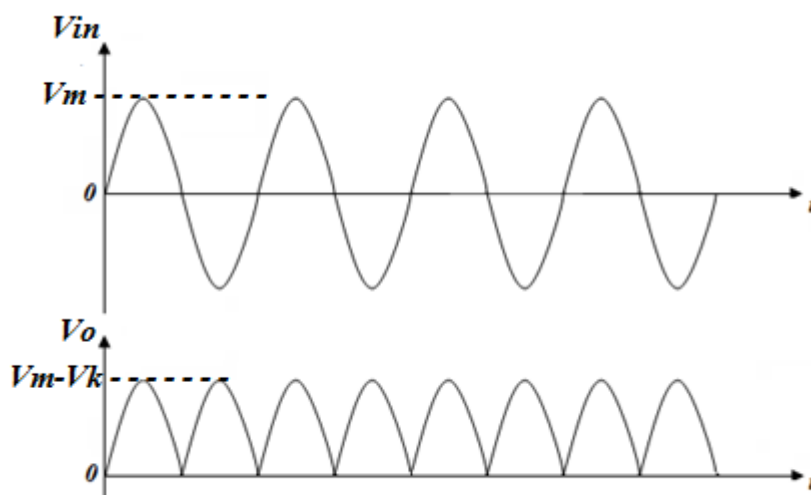


Fig 9(B).1.b Wave forms of Full wave rectifier.

TABULAR COLUMN

$R_L(\text{ohms})$	$I_{dc}(\text{mA})$	$V_{dc}(\text{V})$	$V_{ac}(\text{V})$	$I_{ac}(\text{mA})$	Efficiency % η	Ripple $\gamma = V_{ac}/V_{dc}$	Regulation %R

Table 9(B).1.a To record the experimental values of Half wave rectifier.

9(B).2 FULL WAVE RECTIFIER WITH CAPACITOR FILTER

CIRCUIT DIAGRAM

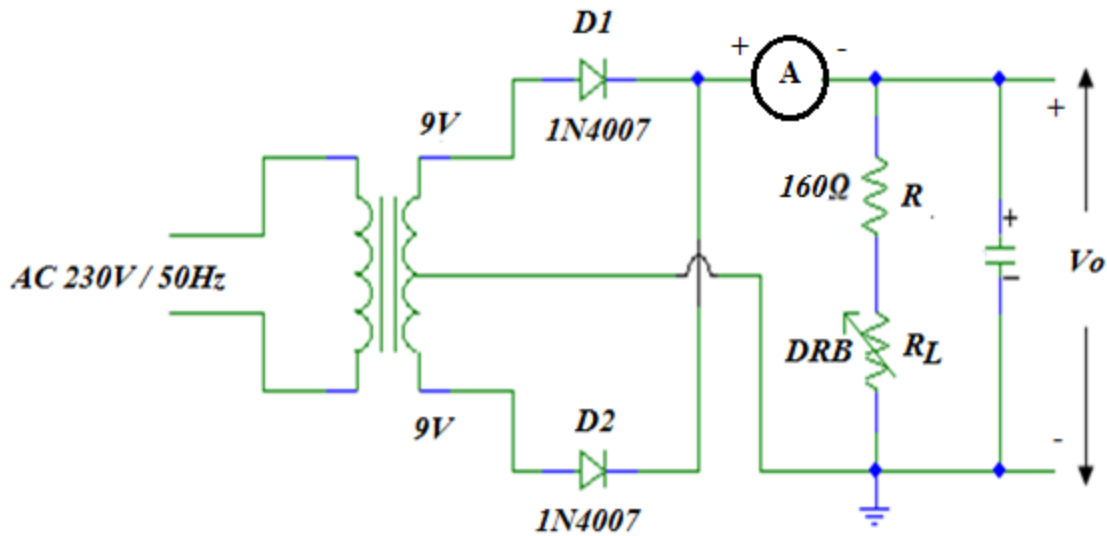


Fig 9(B).2.a Full wave rectifier circuit with capacitor filter.

DESIGN

Let output DC voltage and current required i.e, $V_{dc}=5V$ and $I_{dc}=I_{L(max)}=50mA$ respectively.

Output voltage DC voltage is given by $V_{dc} = I_{dc} R_L$

So $R_L = V_{dc} / I_{dc} = 8V / 50mA = 160\Omega$

Power dissipated in R_L is , $P_L = V_{dc} I_{L(max)} = 8 \times 50 \times 10^{-3} = 0.4 \text{ Watts}$

For R_L use $160\Omega/0.5W$ in series with DRB

For Half wave rectifier , $V_{dc} = 2V_m / \pi$

$V_m = V_{dc} \pi / 2 = 8\pi / 2 = 12.56V$ Where V_m = peak value of transformer secondary voltage

$V_{rms} = V_m / \sqrt{2} = 12.56 / \sqrt{2}$ Where V_{rms} = peak value of transformer secondary voltage

$$\Rightarrow V_{rms}=9V$$

Select 9V secondary (9V-0-9V transformer)

DESIGN FOR THE CAPACITOR FILTER

Let ripple factor $\gamma=0.04$

Ripple = $1 / 4\sqrt{3}fRC$, we have $f=50\text{Hz}$

Therefore $C = 1 / (4 \times \sqrt{3} \times 50 \times 160 \times 0.04) = 451\mu\text{F}$

Use $C=500\mu\text{F}$ a standard value

FORMULAE

DC Output Power , $P_{dc} = (I_{dc})^2 R_L$

AC Input Power , $P_{ac} = [(I_{rms})^2 \times (R_L + R_F)]$, Where R_F is diode forward resistance

Assume $R_F=10\Omega$

Efficiency $\eta = \text{Output DC power} / \text{Input AC power}$

$\% \eta = (P_{dc} / P_{ac}) \times 100$

$\% \text{ Regulation} = [(V_{dc(NL)} - V_{dc(FL)}) / V_{dc(FL)}] \times 100$

Ripple factor $\gamma = V_{ac} / V_{dc}$ or I_{ac} / I_{dc}

PROCEDURE

1. Test the transformer and observe the secondary waveform in CRO.
2. Connect circuit the secondary as shown in the Fig 9(B).2.a.
3. Observe the waveform on CRO across the load resistor which appears as in fig given below.
4. Set the DRB(Load Resistance) to maximum and note down value of currents I_{dc} and I_{ac} with the same multimeter (using proper ranges and modes(i.e, AC or DC)). Also note down the value of voltages V_{dc} and V_{ac} with the same multimeter (using proper ranges and modes). The value of V_{dc} for DRB set to maximum is designated as $V_{dc(NL)}$ (No Load Voltage).
5. Vary I_{dc} in steps by varying DRB and measure corresponding values of I_{dc} , V_{dc} , V_{ac} and record the readings as shown in Table 9(B).2.a .
6. Measure V_m from CRO ($V_{dc}=V_m / \pi$).
7. Measure V_{ac} across the load.
8. Find ripple = V_{ac} / V_{dc} .
9. Measure I_{dc} and I_{rms} .
10. Find efficiency $\% \eta$.

11. Open circuit the load and measure no load voltage $V_{dc(NL)}$ (i.e, set DRB to maximum).
12. Measure full load Voltage $V_{dc(FL)}$ (i.e, set DRB to some low resistance 100Ω , 200Ω etc).
13. Find the percentage regulation %R.
14. Calculate the Ripple Factor and Efficiency for each load resistance.

OUTPUT WAVEFORMS

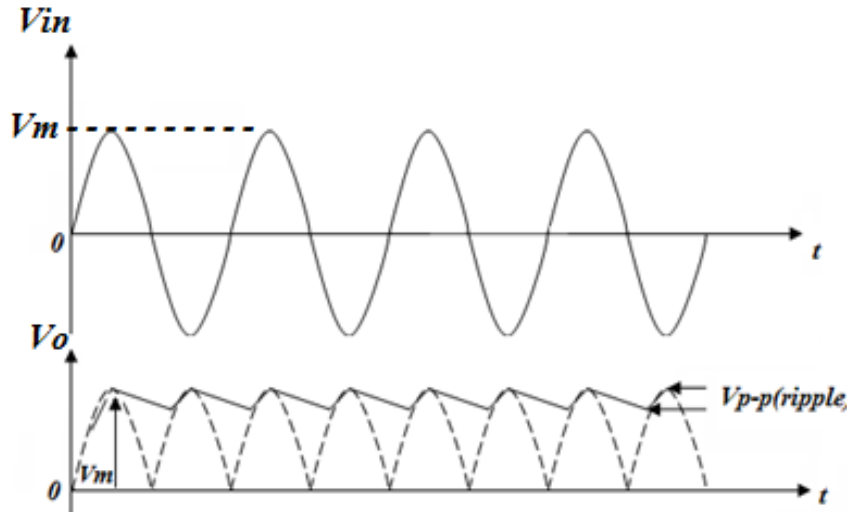


Fig 9(B).2.b Wave forms of Full wave rectifier with capacitor filter.

TABULAR COLUMN

$R_L(\text{ohms})$	$I_{dc}(\text{mA})$	$V_{dc}(\text{V})$	$V_{ac}(\text{V})$	$I_{ac}(\text{mA})$	Efficiency % η	Ripple $\gamma = V_{ac}/V_{dc}$	Regulation %R

Table 9(B).2.a to record the experimental values of Half wave rectifier with capacitor filter.

$$V_{DC} = V_m - (V_{p-p} \text{ Ripple} / 2)$$

$$V_{rms} = V_{p-p} \text{ Ripple} / 2\sqrt{3}$$

RESULT

	Ripple factor value	Efficiency	Regulation
FWR -center tap without filter			
FWR -center tap with filter			

OBSERVATION AND WORK SHEET

9(C) BRIDGE RECTIFIER

AIM

To study full wave rectifier circuit with and without filter and to calculate ripple factor and efficiency.

COMPONENTS REQUIRED

Sl. No	Apparatus	Range	Quantity
01	Bread board		1
02	Diode	1N4007	4
03	Capacitor	47 μ F	1
04	VRPS	0-30V DC ,3A	1
05	CRO for testing		1
06	Probes, wires		1
07	Digital multimeter		1
08	DRB		1

THEORY

A rectifier converts ac to pulsating dc. Rectifiers are used in the design of dc power supplies required for all electrical circuits to work. A semiconductor diode conducts only in one direction. This property is used in the design of rectifier circuit. Based on the output there are mainly two types of rectifiers namely half wave and full wave rectifiers. As the Dc output voltage is in pulsed form, capacitor is used to filter it.

Bridge rectifier is essentially a full wave rectifier circuit, using four diodes, forming the four arms of an electrical bridge . To one diagonal of the bridge the ac voltage is applied through the transformer and the rectified dc voltage is taken from the other diagonal of the bridge. The main advantage of this circuit is that it does not require a center tap on the secondary winding of the transformer; ac voltage can be directly applied to the bridge.

The bridge rectifier circuits are normally used as power rectifier circuit for converting ac power to dc power and a rectifying system in the rectifier type ac meters, such as ac voltmeter in which the ac voltage under measurement is first covered into dc and measured with conventional meter

9(C).1 BRIDGE RECTIFIER WITHOUT CAPACITOR FILTER

CIRCUIT DIAGRAM

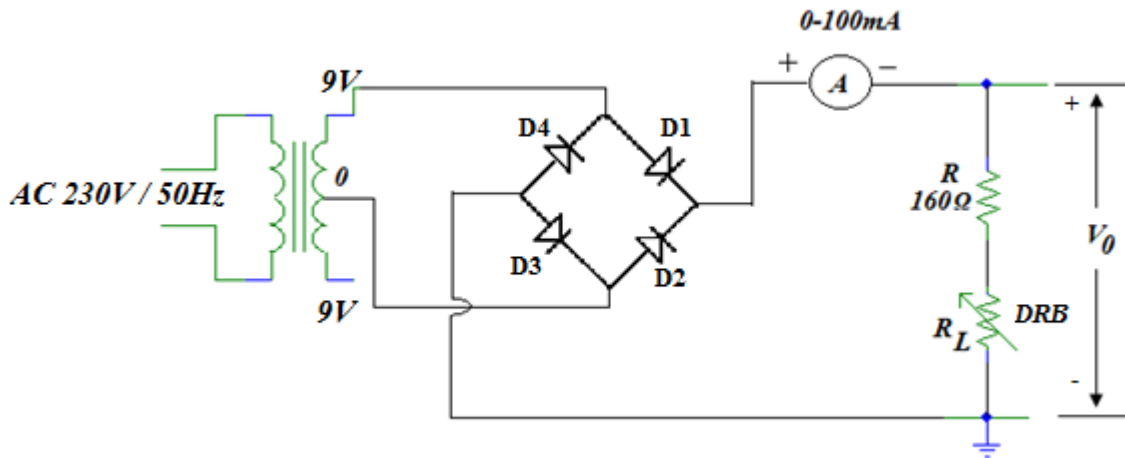


Fig 9(C).1.a Full wave bridge rectifier.

DESIGN

Let output DC voltage and current required i.e, $V_{dc}=5V$ and $I_{dc}=I_{L(max)}=50mA$ respectively.

Output voltage DC voltage is given by $V_{dc} = I_{dc} R_L$

So $R_L = V_{dc} / I_{dc} = 8V / 50mA = 160\Omega$

Power dissipated in R_L is , $P_L = V_{dc} I_{L(max)} = 8 \times 50 \times 10^{-3} = 0.4 \text{ Watts}$

For R_L use $160\Omega/0.5W$ in series with DRB

For Half wave rectifier , $V_{dc} = 2V_m / \pi$

$V_m = V_{dc} \pi / 2 = 8\pi / 2 = 12.56V$ Where V_m = peak value of transformer secondary voltage

$V_{rms} = V_m / \sqrt{2} = 12.56 / \sqrt{2}$ Where V_{rms} = peak value of transformer secondary voltage

$\Rightarrow V_{rms}=9V$

Select 9V secondary (9V-0-9V transformer)

FORMULAE

DC Output Power , $P_{dc} = (I_{dc})^2 R_L$

AC Input Power , $P_{ac} = [(I_{rms})^2 * (R_L + 2R_F)]$, Where R_F is diode forward resistance

Assume $R_F = 10\Omega$

Efficiency η = Output DC power / Input AC power

$\% \eta = (P_{dc} / P_{ac}) * 100$

$\% \text{ Regulation} = [(V_{dc(NL)} - V_{dc(FL)} / V_{dc(FL)}] * 100$

Ripple factor $\gamma = V_{ac} / V_{dc}$ or I_{ac} / I_{dc}

PROCEDURE

1. Test the transformer and observe the secondary waveform in CRO.
2. Connect circuit the secondary as shown in the Fig 9(C).1.a.
3. Observe the waveform on CRO across the load resistor which appears as in fig given below.
4. Set the DRB(Load Resistance) to maximum and note down value of currents I_{dc} and I_{ac} with the same multimeter (using proper ranges and modes(i.e, AC or DC). Also note down the value of voltages V_{dc} and V_{ac} with the same multimeter (using proper ranges and modes). The value of V_{dc} for DRB set to maximum is designated as $V_{dc(NL)}$ (No Load Voltage).
5. Vary I_{dc} in steps by varying DRB and measure corresponding values of I_{dc} , V_{dc} , V_{ac} and record the readings as shown in Table 9(C).1.a .
6. Measure V_m from CRO ($V_{dc} = V_m / \pi$).
7. Measure V_{ac} across the load.
8. Find ripple = V_{ac} / V_{dc} .
9. Measure I_{dc} and I_{rms} .
10. Find efficiency $\% \eta$.
11. Open circuit the load and measure no load voltage $V_{dc(NL)}$ (i.e, set DRB to maximum).
12. Measure full load Voltage $V_{dc(FL)}$ (i.e, set DRB to some low resistance 100Ω , 200Ω etc).

13. Find the percentage regulation %R.

14. Calculate the Ripple Factor and Efficiency for each load resistance.

WAVEFORMS

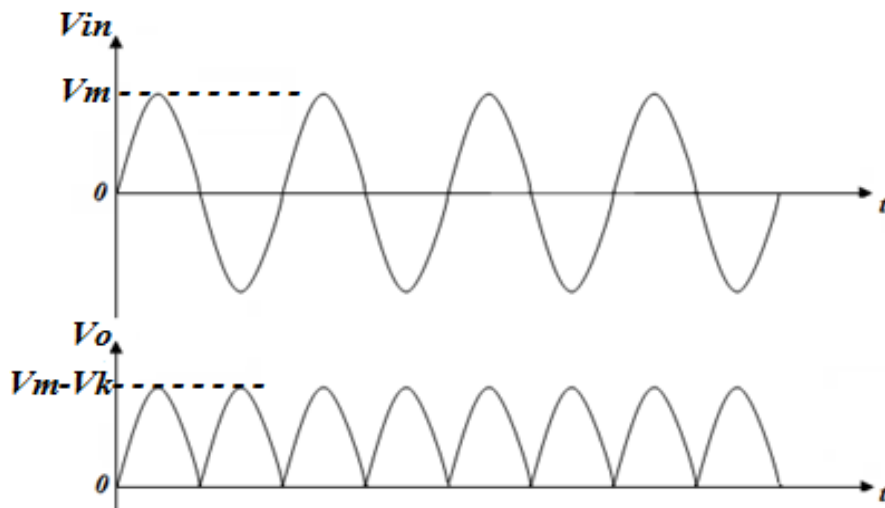


Fig 9(C).1.b Waveforms of bridge rectifier.

TABULAR COLUMN

$R_L(\text{ohms})$	$I_{dc}(\text{mA})$	$V_{dc}(\text{V})$	$V_{ac}(\text{V})$	$I_{ac}(\text{mA})$	Efficiency % η	Ripple $\gamma = V_{ac}/V_{dc}$	Regulation %R

Table 9(C).1.a To record experimental values of bridge rectifier.

9(C).2 FULL WAVE BRIDGE RECTIFIER WITH CAPACITOR FILTER

CIRCUIT DIAGRAM

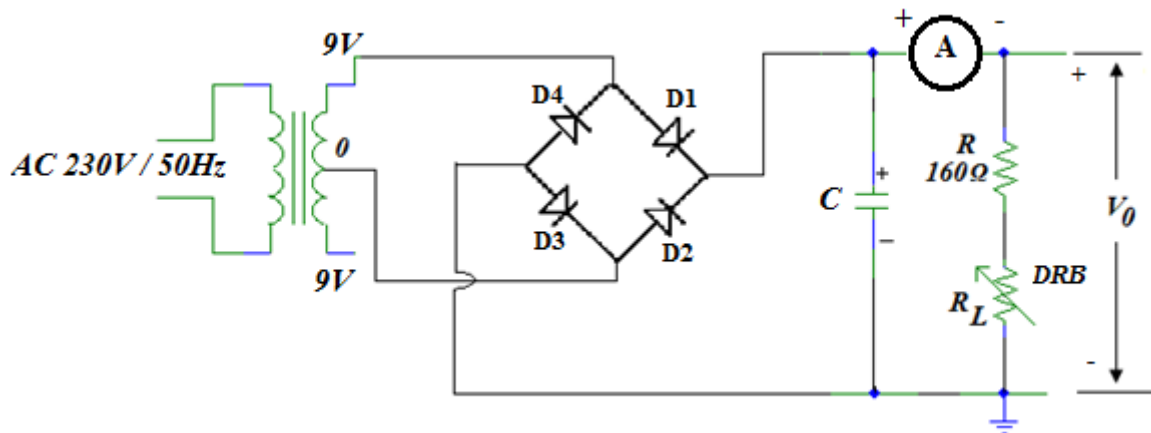


Fig 9(C).2.a Full wave bridge rectifier with capacitor filter.

DESIGN

Let output DC voltage and current required i.e, $V_{dc}=5V$ and $I_{dc}=I_{L(max)}=50mA$ respectively.

Output voltage DC voltage is given by $V_{dc} = I_{dc} R_L$

So $R_L = V_{dc} / I_{dc} = 8V / 50mA = 160\Omega$

Power dissipated in R_L is, $P_L = V_{dc} I_{L(max)} = 8 \times 50 \times 10^{-3} = 0.4 \text{ Watts}$

For R_L use $160\Omega/0.5W$ in series with DRB

For Half wave rectifier, $V_{dc} = 2V_m / \pi$

$V_m = V_{dc} \pi / 2 = 8\pi / 2 = 12.56V$ Where V_m = peak value of transformer secondary voltage

$V_{rms} = V_m / \sqrt{2} = 12.56 / \sqrt{2}$ Where V_{rms} = peak value of transformer secondary voltage

$$\Rightarrow V_{rms}=9V$$

Select 9V secondary (9V-0-9V transformer)

DESIGN FOR THE CAPACITOR FILTER

Let ripple factor $r=0.04$

Ripple = $1 / 4\sqrt{3}fRC$, we have $f=50Hz$

Therefore $C = 1 / (4 \times \sqrt{3} \times 50 \times 160 \times 0.04) = 451\mu F$

Use $C=500\mu F$ a standard value

FORMULAE

DC Output Power , $P_{dc} = (I_{dc}^2 * R_L)$

AC Input Power , $P_{ac} = [(I_{rms})^2 * (R_L + 2R_F)]$, Where R_F is diode forward resistance

Assume $R_F=10\Omega$

Efficiency η = Output DC power / Input AC power

$\% \eta = (P_{dc} / P_{ac}) * 100$

$\% \text{ Regulation} = [(V_{dc(NL)} - V_{dc(FL)} / V_{dc(FL)}] * 100$

Ripple factor $\gamma = V_{ac} / V_{dc}$ or I_{ac} / I_{dc}

PROCEDURE

1. Test the transformer and observe the secondary waveform in CRO.
2. Connect circuit the secondary as shown in the Fig 9(C).2.a.
3. Observe the waveform on CRO across the load resistor which appears as in fig given below.
4. Set the DRB(Load Resistance) to maximum and note down value of currents I_{dc} and I_{ac} with the same multimeter (using proper ranges and modes(i.e, AC or DC). Also note down the value of voltages V_{dc} and V_{ac} with the same multimeter (using proper ranges and modes). The value of V_{dc} for DRB set to maximum is designated as $V_{dc(NL)}$ (No Load Voltage).
5. Vary I_{dc} in steps by varying DRB and measure corresponding values of I_{dc} , V_{dc} , V_{ac} and record the readings as shown in Table 9(C).2.a .
6. Measure V_m from CRO ($V_{dc}=V_m / \pi$).
7. Measure V_{ac} across the load.
8. Find ripple = V_{ac} / V_{dc} .
9. Measure I_{dc} and I_{rms} .
10. Find efficiency $\% \eta$.
11. Open circuit the load and measure no load voltage $V_{dc(NL)}$ (i.e, set DRB to maximum).
12. Measure full load Voltage $V_{dc(FL)}$ (i.e, set DRB to some low resistance 100Ω , 200Ω etc).

13. Find the percentage regulation %R.

14. Calculate the Ripple Factor and Efficiency for each load resistance.

OUTPUT WAVEFORMS

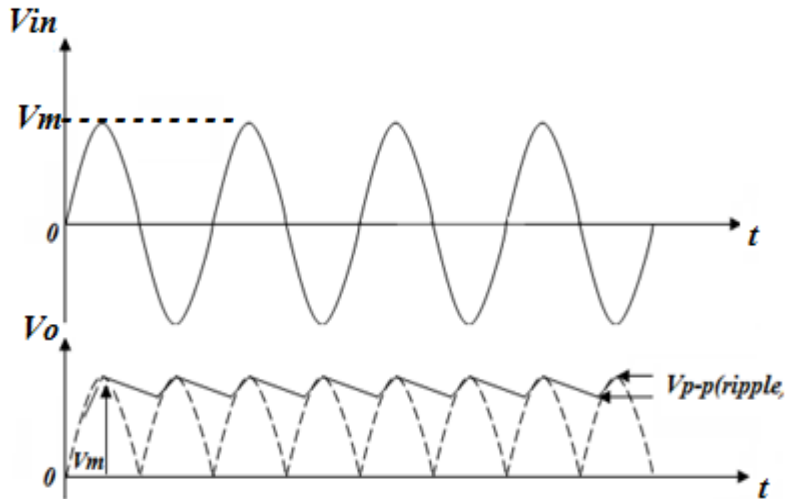


Fig 9(C).2.b Waveforms of bridge rectifier with capacitor filter.

TABULAR COLUMN

$R_L(\text{ohms})$	$I_{dc}(\text{mA})$	$V_{dc}(\text{V})$	$V_{ac}(\text{V})$	$I_{ac}(\text{mA})$	Efficiency $\% \eta$	Ripple $\gamma = V_{ac}/V_{dc}$	Regulation $\% R$

Table 9(C).2.a To record experimental values of bridge rectifier with capacitor filter.

$$V_{DC} = V_m - (V_{p-p} \text{ Ripple} / 2)$$

$$V_{rms} = V_{p-p} \text{ Ripple} / 2\sqrt{3}$$

RESULT

	Ripple factor value	Efficiency	Regulation
Bridge rectifier without c-filter			
Bridge rectifier with c-filter			

EXPECTED VIVA QUESTIONS

1. What is meant by leakage current OR reverse current?
2. What is filter?
3. What is ripple?
4. Classify different types of rectifiers.
5. What is half wave Rectifier?
6. What is full wave Rectifier?
7. What is bridge wave Rectifier?
8. What is the use of capacitor in the rectifier circuit?
9. Mention the efficiency of all the rectifiers.
10. What is regulation?
11. What are the types of regulation?
12. What is load regulation?
13. What is precision rectifier?
14. What is line regulation?
15. Why ordinary diode can't rectify very small voltages?

OBSERVATION AND WORK SHEET

EXPERIMENT NO.10**THEVENIN'S AND MAXIMUM POWER TRANSFER THEOREM****10(A) THEVENIN'S THEOREM****AIM**

To Verify Thevenin's and Maximum Power Transfer Theorem for the given network.

COMPONENTS REQUIRED

Sl. No	Apparatus	Range	Quantity
01	Bread Board		1
02	Ammeter	(0-100)mA	1
03	Resistors	1K Ω	4
04	VRPS	0-30V DC, 3A	
05	Wires		15
06	Digital multimeter		1

THEORY

THEVENIN'S THEOREY: "Any active linear network with two terminals can be replaced by an equivalent voltage source in series with a resistance, the voltage being equal to the open-circuit voltage at the terminals and the resistance being equal to the resistance of the network between the terminals with all voltage sources in the network replaced by their internal resistances"

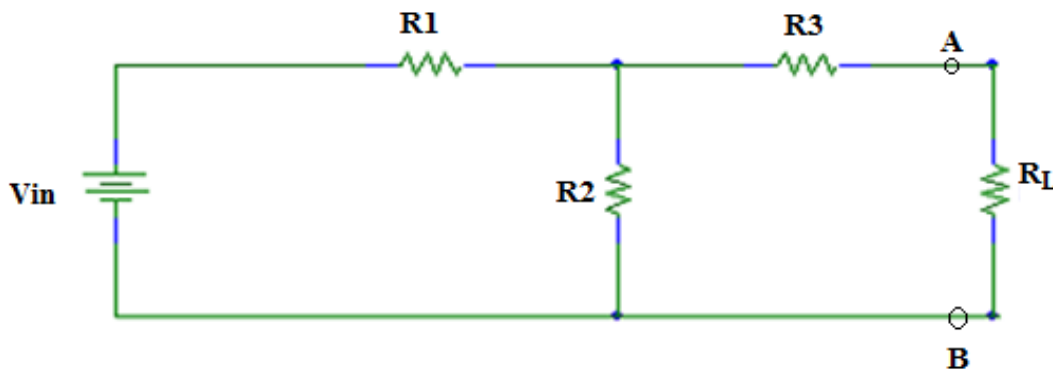
CIRCUIT DIAGRAM

Fig 10(A).1 Circuit diagram to which Thevenin's theorem has to be proved

DESIGN

Let $V_{in}=5V$, $R_1=1K\Omega$, $R_2=1K\Omega$, $R_3=1K\Omega$ and $R_L=1K\Omega$

To find the theoretical value of V_{TH} and R_{TH} for the given circuit

$$R_{TH} = R_1 \parallel R_2 + R_3 \text{ (by open circuiting the terminal AB and short circuiting } V_{in} \text{ as in Fig 10(A).4)}$$

$$= (1K \parallel 1K) + 1K = 1.5K\Omega$$

$$V_{TH} = [R_2 / (R_1 + R_2)] * V_{in} \text{ (using Fig 11(A).3)}$$

$$= [1K / (1K + 1K)] * 5 = 2.5 V$$

After connecting equivalent circuit in fig 11(A).5

$$I_L = V_{TH} / (R_{TH} + R_L) = 2.5 / (1.5K + 1K) = 1mA$$

PROCEDURE

1. Rig up the circuit as shown below and determine the load current I_L .

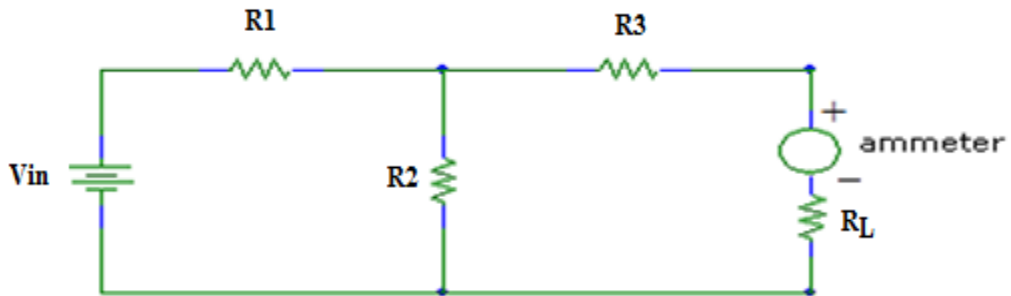


Fig 10(A).2

2. Find Thevenin's voltage by removing the load connected between terminals A and B as shown in the circuit below.

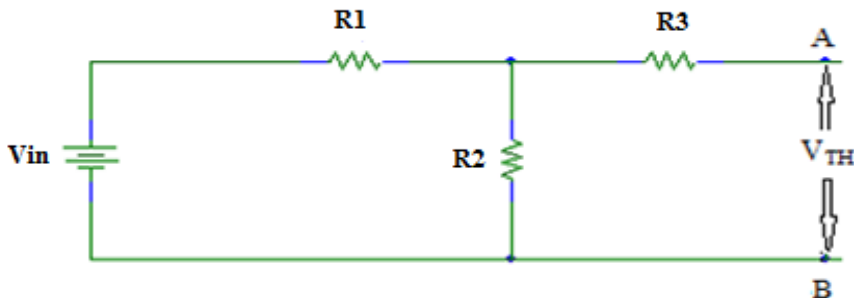


Fig 10(A).3

3. Connect the circuit as shown below and find the thevenin's resistance R_{TH} .

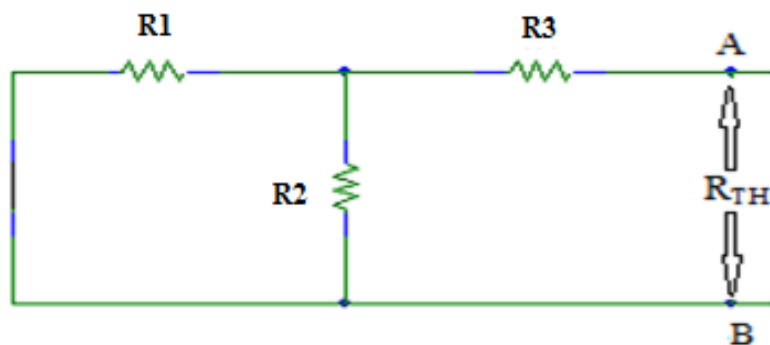


Fig 10(A).4

4. Rig up the thevenins equivalent circuit as shown below and find the Thevenins current I_{th}

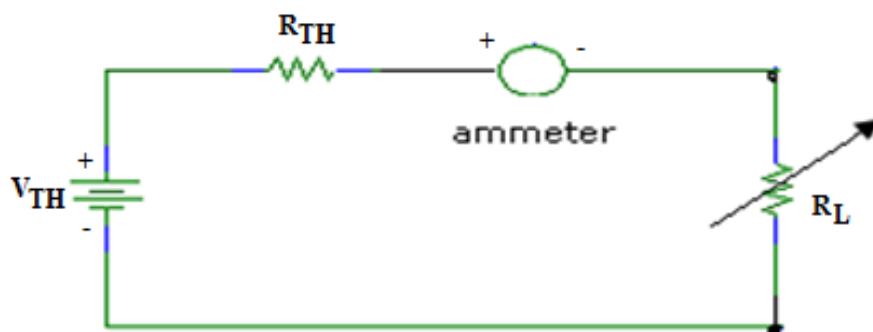


Fig 10(A).5

5. Observe I_{TH} and I_L . If they are equal then Thevenin's theorem is proved.

6.

TABULAR COLUMN

THEORITICAL			PRACTICAL		
V_{TH}	R_{TH}	I_L	V_{TH}	R_{TH}	I_L
2.5V	1.5K Ω	1mA			

Table 10(A).1 To note down the experimental values for Thevenin's theorem

RESULT: Thevenin's theorem is verified

OBSERVATION AND WORK SHEET

10(B) MAXIMUM POWER TRANSFER THEOREM

AIM

To verify Maximum Power Transfer Theorem for the given network.

COMPONENTS REQUIRED

Sl. No	Apparatus	Range	Quantity
01	Bread Board		1
02	Ammeter	(0-100)mA	1
03	Resistors	2.2K Ω , 3.3K Ω , 4.7K Ω , 1K Ω	1
04	VRPS	0-30V DC, 3A	
06	Digital multimeter		1

THEORY

MAXIMUM POWER TRANSFER THEOREM: "The power derived by an active network to a load connected across its terminal is maximum, when the impedance of the load is the complex conjugate of the active network impedance"

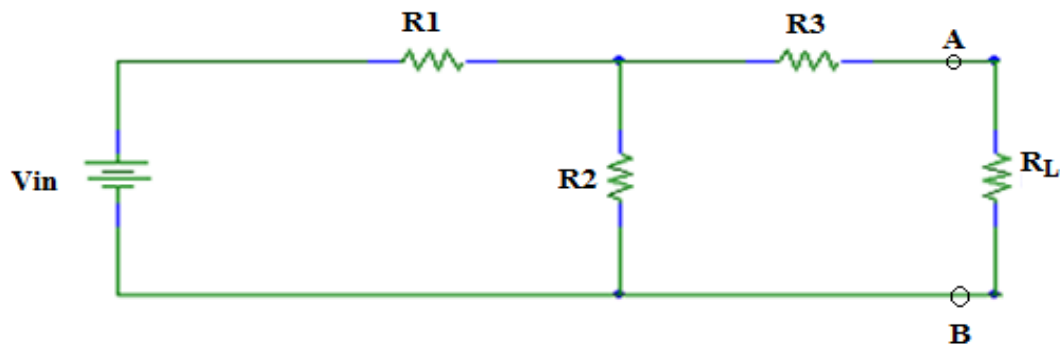
The magnitude of maximum power transferred is given by ,

$$P = I_L^2 \cdot R_L \quad (\text{we have taken a pure resistive circuit to verify the theorem})$$

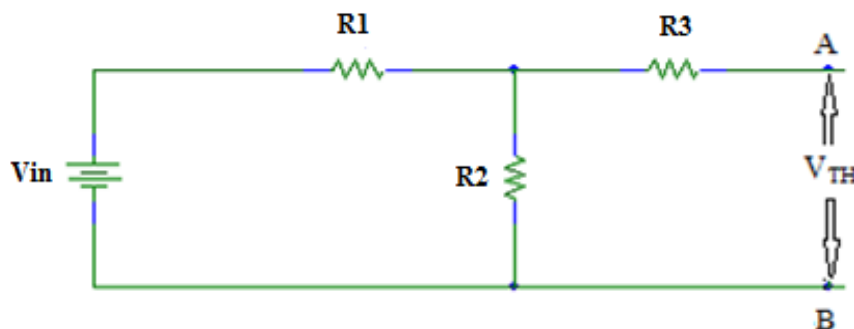
$$= [V_{th}/(R_L + R_{th})^2] \cdot R_L,$$

Where the V_{th} and R_{th} are the Thevenin's Voltage and Resistance found looking back into the network (given circuit) from load by open circuiting load. Now

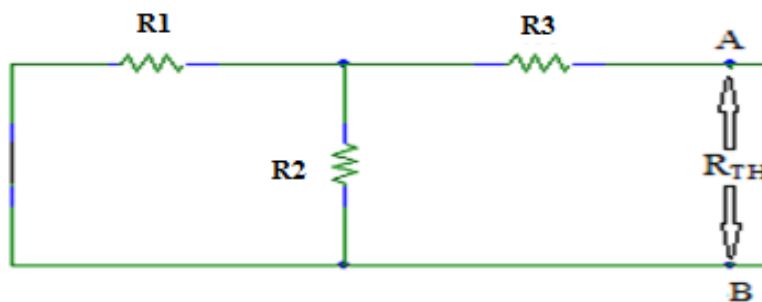
$$P = [V_{th}/(R_L + R_L)^2] \cdot R_L \quad \text{since for maximum power transfer } R_{th} = R_L$$

CIRCUIT DIAGRAM**Fig 10(B).1** Circuit diagram to which Maximum theorem has to be proved**PROCEDURE**

1. First find the thevenin's equivalent circuit for the given circuit as given below
 - (a) Find Thevenin's voltage by removing the load connected between terminals A and B as shown in the circuit below.

**Fig 10(B).2**

- (b) Connect the circuit as shown below and find the thevenin's resistance R_{TH}

**Fig 10(B).3**

- (2). Rig up the Thevenin's equivalent circuit as shown below with Load R_L

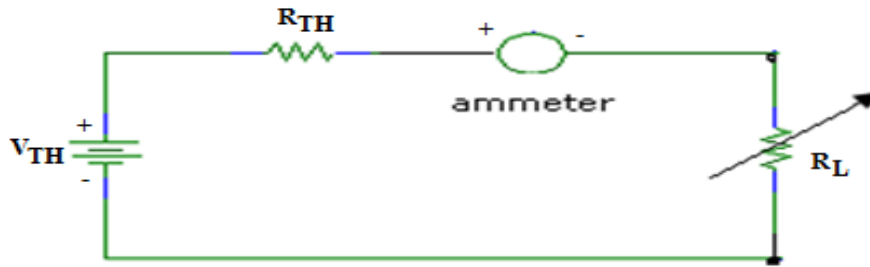


Fig 10(B).4

- (3). Vary the load resistance in appropriate steps and note down the corresponding load current and load voltage.
- (4). Tabulate the readings and find power for each load resistance value.
- (5). Plot the graph of R_L versus Load Power with R_L on X-axis and Power on Y-axis.
- (6). Observe that the maximum power is transferred to the load when R_L is equal to R_{TH} .

EXPECTED GRAPH

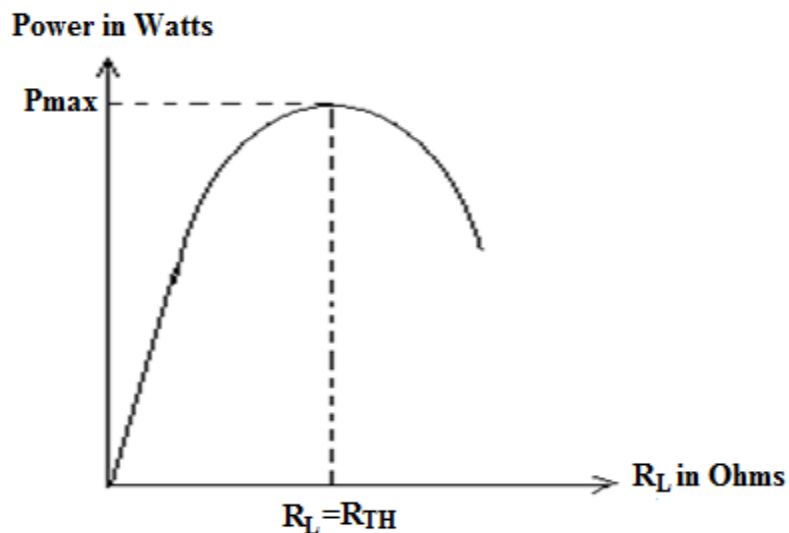


Fig 10(B).2 Output graph of Maximum Power Transfer theorem

TABULAR COLUMN

R_L(ohms)	V_L(Volts)	I_L (mA)	P_L = V_L * I_L(watts)

Table 10(B).1 To record the experimental values for Maximum power transfer theorem

RESULT

For a given circuit, Thevenin's and Maximum Power Transfer Theorems have been designed and verified.

EXPECTED VIVA QUESTIONS

1. Define Thevenin's and Maximum Power Transfer Theorems .
2. Explain the procedure for both the theorems.
3. Explain both the theorems with respect to simple circuit.
4. What type of circuits will satisfy Thevenin's theorem ?
5. What type of circuits will satisfy maximum power transfer theorem?

OBSERVATION AND WORK SHEET

EXPERIMENT NO.11**CHARACTERISTICS OF SERIES & PARALLEL RESONANCE CIRCUIT****11(A) SERIES RESONANCE CIRCUIT****AIM**

To obtain the frequency response of an RLC series resonant circuit and to determine resonance frequency.

COMPONENTS REQUIRED

Sl. No	Apparatus & components	Range	Quantity
01	Bread board		1
02	Variable inductance		DRB
03	Variable resistors		DRB
04	Variable Capacitors		DRB
05	Signal generator	10Hz to 1Mhz	1
06	Ammeter	(0-100)mA	1
07	CRO for testing		1
08	Probes, wires		2+15
09	Multimeter for testing		1

THEORY

A circuit is said to be under resonance if the current flowing in the circuit is in phase with the applied voltage, that is if the whole circuit acts like a pure resistive circuit, and the circuit current will be in phase with the voltage.

Resonance is a phenomenon that occurs in AC circuits, when an inductance coil and capacitance are connected in series across an alternating supply of varying frequency. Resonance condition can be achieved either by keeping network elements same and varying frequency or by keeping frequency same and varying the frequency dependent circuit elements.

CIRCUIT DIAGRAM

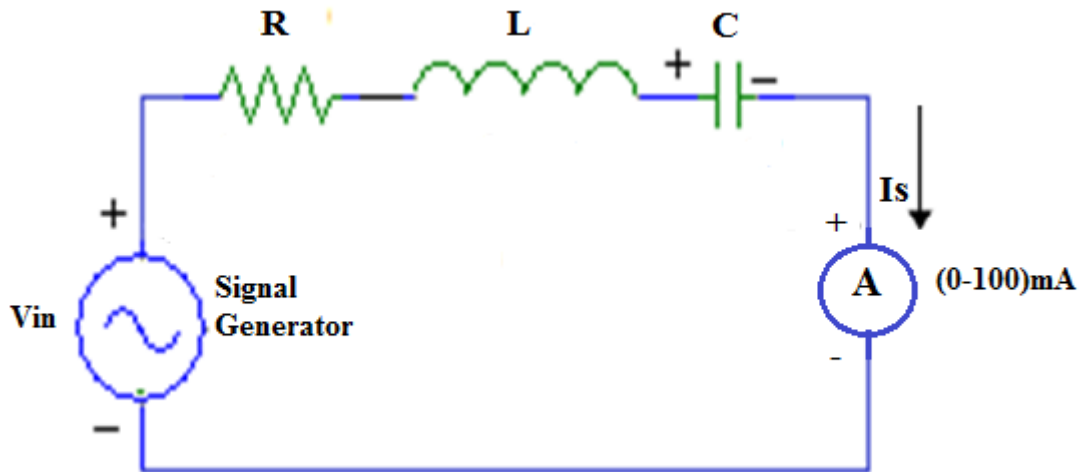


Fig 11(A).1 Circuit diagram of series resonance circuit

DESIGN

Theoretical Series Resonant is given by the equation,

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Let $f_0 = 35 \text{ KHz}$ and assume $R = 100\Omega$, $L = 1\text{mH}$.

The value of C is given by

$$35 \times 10^3 = \frac{1}{2\pi\sqrt{1 \times 10^{-3} \times C}} \Rightarrow C = 0.021\mu\text{F}; \text{ Use } C = 0.022\mu\text{F}$$

Quality factor is given by $Q = X_L / R = \omega_0 L / R$

Or

$$Q = X_C / R = 1 / \omega_0 C R \text{ or } Q = f_0 / BW$$

Bandwidth is given by, $BW = f_0 / Q$ or $BW = f_0 / (f_H - f_L)$

PROCEDURE

1. For Series resonance, rig up the circuit as shown in the circuit diagram 11(A).1 and set the input voltage constant at $20V_{(p-p)}$ at 100Hz.
2. Now vary the input frequency from 100Hz to 100KHz and note down the value of corresponding series current I_s shown by the ammeter A for each frequency.

- ## TABULAR COLUMN

Table 11(A).1 To record the experimental values of series resonance circuit

EXPECTED FREQUENCY RESPONSE

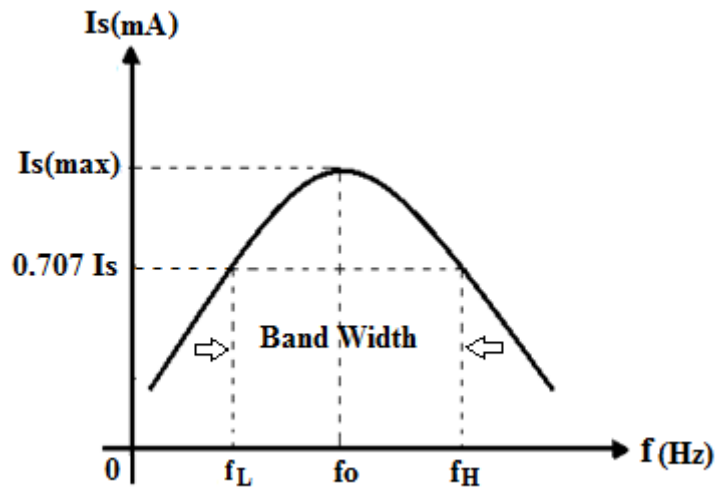


Fig 11(A).2 Graph of Current versus Frequency

RESULT

1. Theoretical series resonant frequency $f_0 = \underline{\hspace{2cm}}$ KHz
2. Practical series resonant frequency $f_0 = \underline{\hspace{2cm}}$ KHz
3. Lower cut-off frequency $f_L = \underline{\hspace{2cm}}$ KHz
4. Upper cut-off frequency $f_H = \underline{\hspace{2cm}}$ KHz
5. Band Width $BW = (f_H - f_L) = \underline{\hspace{2cm}}$ KHz

11(B) PARALLEL RESONANCE CIRCUIT**AIM**

To obtain the frequency response of an RLC parallel resonant circuit and to determine resonance frequency.

COMPONENTS REQUIRED

Sl. No	Apparatus & components	Range	Quantity
01	Bread board		1
02	Variable inductance		
03	Variable resistors		
04	Variable Capacitors		
05	Signal generator	10Hz to 1MHz	1
06	CRO for testing		1
07	Probes, wires		2+15
08	Multimeter for testing		1

THEORY

A circuit is said to be under resonance if the current flowing in the circuit is in phase with the applied voltage that is if the whole circuit acts like a pure resistive circuit, and the circuit current will be in phase with the voltage.

Resonance is a phenomenon and study of AC circuits, when an inductance coil and capacitance are connected in parallel across an alternating supply of varying frequency. Resonance condition can be achieved either by keeping network elements same and varying frequency or by keeping frequency same and varying the frequency dependent circuit elements.

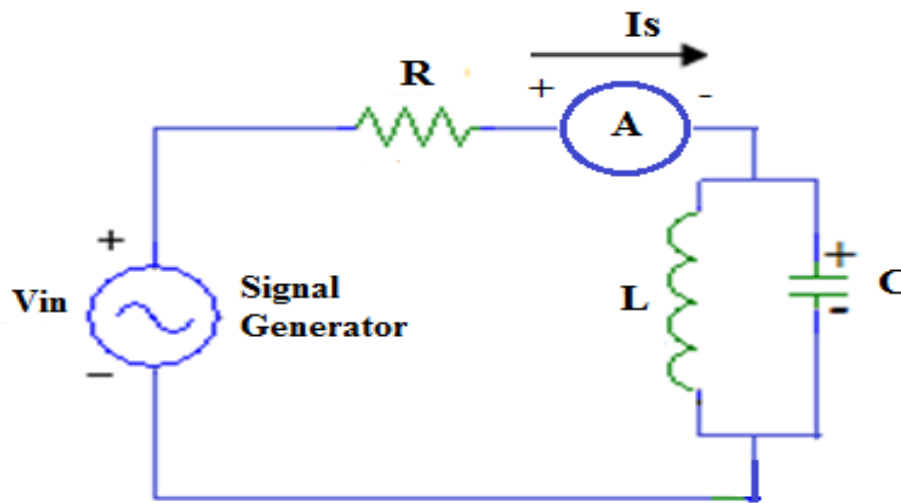
CIRCUIT DIAGRAM

Fig 11(B).1 Circuit diagram of parallel resonance circuit

DESIGN

Theoretical Parallel Resonant circuit shown above is given by the equation,

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Let $f_0 = 35 \text{ KHz}$ and assume $R = 100\Omega$, $L = 1\text{mH}$.

The value of C is given by

$$35 \times 10^3 = \frac{1}{2\pi\sqrt{1 \times 10^{-3} \times C}} \Rightarrow C = 0.021\mu\text{F}; \text{ Use } C = 0.022\mu\text{F}$$

Bandwidth is given by, $BW = f_0 / Q$ or $BW = f_0 / (f_H - f_L)$

Quality factor is given by $Q = f_0 / BW$

PROCEDURE

1. For Parallel resonance, rig up the circuit as shown in the circuit diagram 11(B).1 and set the input voltage constant at $20V_{(p-p)}$ at 100Hz .
2. Now vary the input frequency from 100Hz to 100KHz and note down the value of corresponding series current I_s shown by the ammeter A for each frequency.
3. Current I_s will be minimum at resonant frequency. Record the readings as shown in the tabular column 11(B).1.

- ## EXPECTED FREQUENCY RESPONSE



Frequency in Hz	Is in mA

RESULT

1. Theoretical Parallel resonant frequency $f_0 = \underline{\hspace{2cm}}$ KHz
2. Practical Parallel resonant frequency $f_0 = \underline{\hspace{2cm}}$ KHz
3. Lower cut-off frequency $f_L = \underline{\hspace{2cm}}$ KHz
4. Upper cut-off frequency $f_H = \underline{\hspace{2cm}}$ KHz
5. Band Width $BW = (f_H - f_L) = \underline{\hspace{2cm}}$ KHz

EXPECTED VIVA QUESTIONS

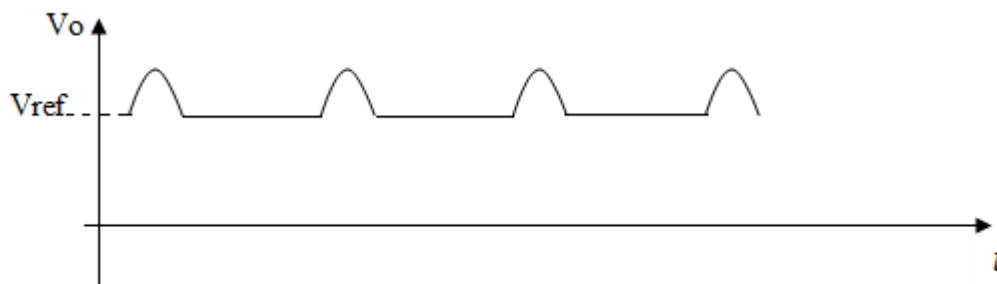
1. Define series resonance.
2. Define parallel resonance.
3. Differentiate between series and parallel resonance circuits.
4. Define quality factor.
5. Define bandwidth.
6. What do you mean by half power frequency?
7. What is the power gain of series resonant circuit?
8. What are the applications of resonant circuits ?.

OBSERVATION AND WORK SHEET

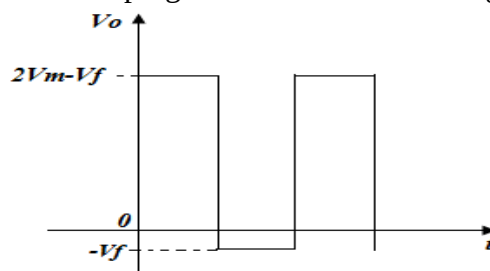
2 GRAPH SHEETS TO BE INSERTED

MODEL QUESTION BANK

- 1) Design RC coupled Single stage BJT/FET amplifier and determine gain – frequency response, input and output impedance
- 2) Design of BJT Darlington Emitter follower with and without bootstrapping and determine gain, input and output impedances
- 3) Design of a two stage FET / BJT voltage feedback amplifier and determine gain, input and output impedances
- 4) Design and testing for the performance of BJT – RC phase shift Oscillator for $f_o \leq 10\text{kHz}$
- 5) Design and testing for the performance of BJT Hartley Oscillator for RF range $f_o \geq 100\text{ kHz}$
- 6) Design and testing for the performance of BJT Colpitts Oscillator for RF range $f_o \geq 100\text{ kHz}$
- 7) Design and testing for the performance of BJT Crystal Oscillator
- 8) Design and construct suitable Diode clipping to obtain the following wave form. Given reference voltages $V_{\text{ref}} = 2\text{volts}$

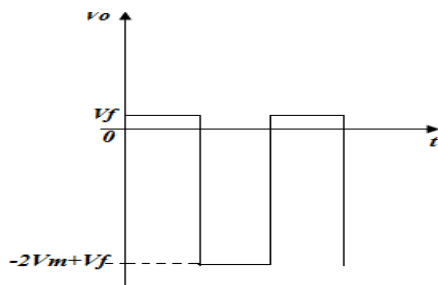


- 9) Design and construct suitable Diode clamping to obtain the following wave form. Given reference



voltages $V_{\text{ref}} = 1\text{volts}$ and $V_m = 8\text{v}$

- 10) Design and construct suitable Diode clamping to obtain the following wave form. Given reference voltages $V_{ref} = 2\text{volts}$ and $V_m = 8\text{v}$



- 11) Design and testing of a Class B push pull amplifier and determination of its conversion efficiency.
- 12) Half wave Rectifier with and without filter. Determine ripple factor, efficiency and Voltage Regulation
- 13) Design Full wave Rectifier with and without filter
- 14) Design Bridge wave Rectifier with and without filter
- 15) Verification of Thevinins and Maximum power transfer theorem
- 16) (a) Verify the Characteristics of Series resonant circuits
- (b) Verify the Characteristics of Parallel resonant circuits